A COMPUTER CONTROLLED SYSTEM FOR TESTING AN INTEGRATED CIRCUIT AUTOMATIC WASHER TIMER

A THESIS

Presented to

The Faculty of the Division of Graduate

Studies and Research

By

Stephen Wayne Vogt

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

Georgia Institute of Technology

October, 1972

A COMPUTER CONTROLLED SYSTEM FOR TESTING

AN INTEGRATED CIRCUIT AUTOMATIC WASHER TIMER

Approved:

J. H. Schlag, Chairman

M. P. Moad

H. N. Nunnally

Date approved by Chairman: ____

ACKNOWLEDGMENTS

I would like to express my greatest appreciation to Dr. J. H. Schlag, my advisor and reading committee chairman, for his constant guidance and assistance in performing the experimentation necessary for my thesis project as well as in preparing this thesis. I would also like to thank the other members of my reading committee, Dr. M. F. Moad and Dr. H. N. Nunnally.

For financial and technical support, I would like to express my profound gratitude to the Whirlpool Corporation and in particular to Ed Getz, Jerry Schornhorst, Jack Clearman, and Jim Ruspino.

Finally an expression of appreciation goes to Mr. R. M. Ford of the School of Electrical Engineering Shop, for his help in hardware fabrication, and to my wife and typist, Betsy.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

SUMMARY

In cooperation with the Whirlpool Corporation, the research described in this thesis was performed to develop a computer controlled system to test an automatic washer electronic timer. The purpose of the electronic timer is to replace the mechanical timer, now used in all clothes washers, with a much more flexible and reliable control unit. The principal part of the entire electronic timer is a metal oxide semiconductor (MOS), large scale integrated circuit developed by North American Rockwell. Because the integrated circuit will be used in a mass produced consumer item which must be reliable, the washer manufacturer requires a system to thoroughly test the integrated circuit in minimum time before it goes into the washer.

The testing system was built around the NOVA 1200 which is a small general purpose computer. In order to control and monitor an external device, the computer requires a basic interface along with any special interfacing necessary to run the device. The purpose of the basic interface is to control the flow of data to and from the computer and a particular external device. The purpose of the special interfacing for the MOS device is to translate the input and output levels and to provide power and a clock pulse.

In the automatic washer, the MOS device uses an external

60 hertz reference frequency as a timing basis to step the washer through a preselected cycle which consists of a specific sequence of functions. Therefore the testing procedure is set up to input every possible cycle and determine if the function sequencing and timing is correct. To speed the testing, the reference frequency is set at its maximum. The computer program provides decision making capabilities to check the functions as they change and contains a loop to check the time duration of each function.

The resultant testing system thoroughly and accurately tests the MOS device. However, the system is limited because of the very long time required to test a device. Since little information on the actual device design is available, the device can only be tested using the input-output relationships. Also the number of different possible cycles is large and the reference frequency is limited by internal synchronization problems. For example, with the maximum reference frequency of 2000 hertz, a 25 minute cycle, one of about 4800 cycles, takes 45 seconds to test. Hence, although this system is limited, it demonstrates the feasibility of testing the MOS device with computer control.

CHAPTER I

INTRODUCTION

The Problem

In cooperation with the Whirlpool Corporation, the research described in this thesis was performed to develop a computer controlled system to test an automatic washer electronic timer. The purpose of the electronic timer is to replace the mechanical timer in the clothes washer with a much more flexible and reliable control unit. The project to replace the mechanical timer was initiated around the end of 1970 and since then the electronic timer has been designed and fabricated, and is in the evaluation stage.

The principal part of the entire electronic timer is a metal oxide semiconductor (MOS), large scale integrated circuit developed by North American Rockwell. Because the integrated circuit will be used in a mass produced consumer item which must be reliable, the washer manufacturer requires a system to thoroughly test the integrated circuit in minimum time before it goes into the washer. Hence, the problem of this research was to design and fabricate such a specialized testing system.

History of the Problem

Although computer controlled integrated circuit testing

is not new in general, it is relatively new in the area of large volume consumer production. Currently Whirlpool engineers are developing a testing procedure for a much less complex integrated circuit used as a timer in the dryer. The dryer integrated circuit is now being tested by a logic comparator which steps a good device and several test devices through all possible inputs and compares the outputs. Although the test is monitored automatically, there is no computer control involved.

The washer manufacturer is using several minicomputers to monitor other types of testing. Life tests on washers, dryers, and on individual machine components such as motors and switches are monitored by computers which shut the machines off in the event of a failure and output information about the cause of the failure. Also dryer efficiency tests, in which the changing weight of the clothes is measured by a load cell, are monitored by a computer which outputs an efficiency curve.

Hence, most of the computer usage for testing purposes is in the area of monitoring rather than controlling. This light usage of computers for testing has proved to be efficient and economical, and has stimulated interest in a computer controlled test procedure for the MOS integrated circuit washer timer.

Literature Review

A literature review revealed that nearly all computer controlled testing is found in the electronics industry as

opposed to the appliance industry or other public type consumer goods industry. Of the ten articles used as references, four are by employees of large instrumentation manufacturers and four are by employees of computer manufacturers or computer consulting firms. The instrumentation manufacturers are naturally very interested in fast, economical testing of their components and systems. Since this comprises the principal market for computer-aided testing, the computer people cater mainly to them. Therefore, there is little available at this time for the appliance manufacturer who wants to test components himself, before they go into his product.

The literature did yield some information on computer controlled or automated testing in general. Bobroff (1) and Cave and Myers (2) compare manual and automatic testing in terms of reliability and economy. Clarke (3) gives some guidelines for determining when a computer is justified for automated testing. McAleer (4) lists nine factors involved in estimating the cost of an automated test program versus a manual test program. Again concerning the economics of computer controlled testing, Michael (5) and Bobroff (1) discuss the advantages of a small dedicated computer over a large central processor, including data transmission considerations.

Fichtenbaum (6) and McAleer (4) emphasize flexibility

in setting up for testing many different circuits and systems. They talk about instrument programmability and compatibility between the computer and the system under test.

Crook and Blythin (7) set up a scheme for synthesizing test patterns to test a device as thoroughly as possible in minimum time. However, they admit the process is sensitive to "unusual" logic on which the scheme will fail. The process is also very limited in the case of large scale integration. Lee (8) discusses the practical aspects of large scale integration testing and infers how to organize a test for such a complex system.

Since electronic circuitry and devices have become so sophisticated, computer controlled testing has become inperative for high reliability and low cost. The introduction of these complex digital devices into appliances and "home" electronics, has now provided a need for computerized testing in the consumer product industry. Not only can the computer handle the complexity, but it can store information about failure and acceptable performance and it can provide decision making capabilities for diagnostics and additional control features. Now the appliance manufacturer must also have a fast, economical means of testing thousands of complex devices whose reliability is very important to his business.

Background

The mechanical timer now used in all automatic washers

consists of a timing motor which turns several rotary cams. The cams are metal disks which operate switches that control the different functions of the washer. These functions include filling with water, agitating, dumping detergent, spinning, and others. Depending on the cycle selected, such as whites or delicates, a specific set of cams is placed in position to control the cycle.* Because of the set rotational speed of the timing motor and the size and number of cams, the mechanical timer is rather limited in its timing and control flexibility. Thus, the need for an electronic timer was evident and the integrated circuit technology was available to make such a project feasible.

The electronic timer consists basically of a metal oxide semiconductor (MOS) integrated circuit with external switches for input or cycle selection and external driver circuits which use the outputs of the MOS device to control the washer functions. A block diagram of the electronic timer as it appears in the washer is shown in Figure 1. More information on the electronic timer and on the MOS device is given in the appendix.

The MOS device itself is made up of (1) a counter, (2) an oscillator, (3) a read only memory (ROM), and (4) other logic necessary to perform the selected functions. Figure 2

*Note: Throughout this paper, the terms cycle and function will be used as given in these examples; a cycle being a broad classification of a specific sequence of functions.

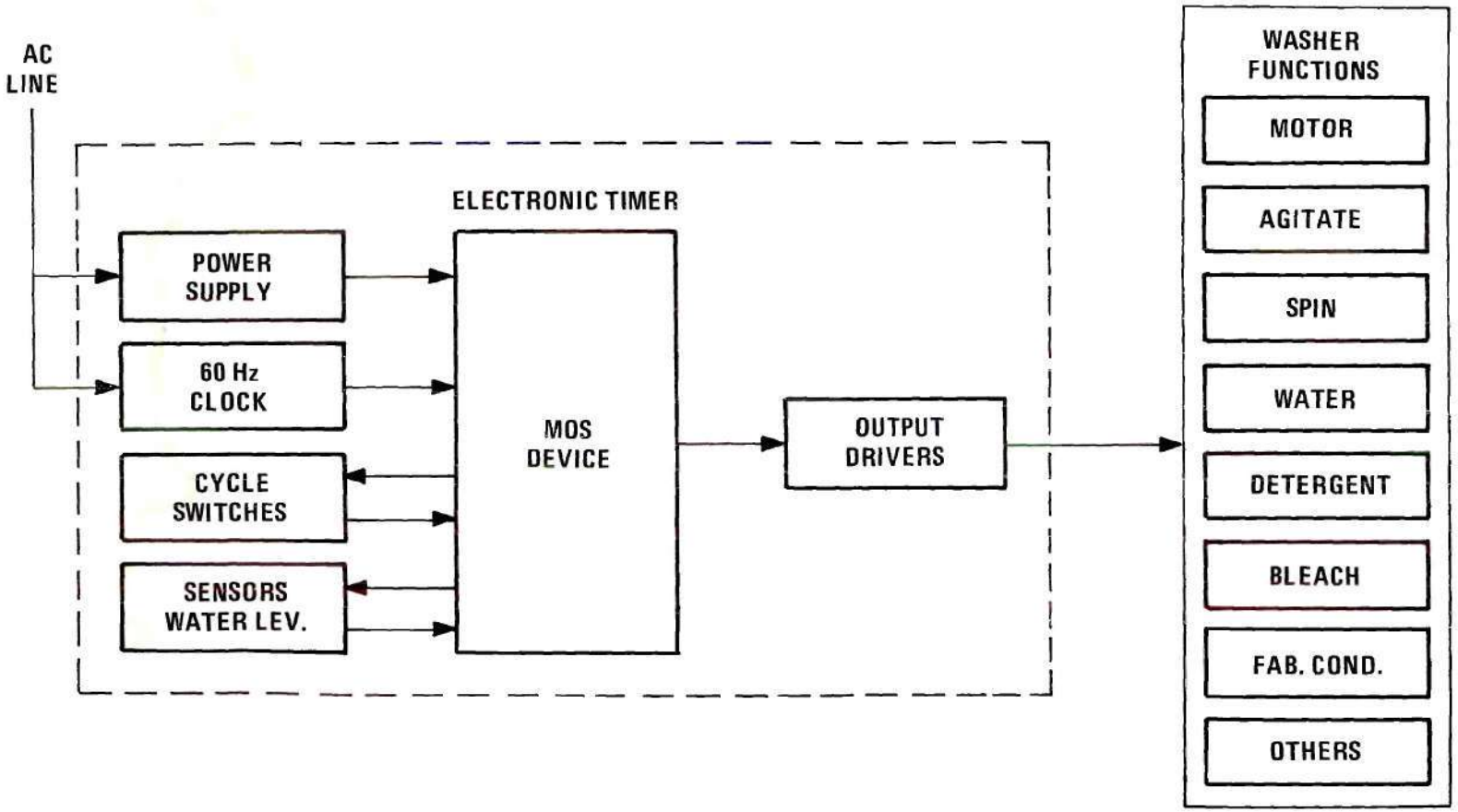


Figure 1. Automatic Washer With Electronic Timer Block Diagram

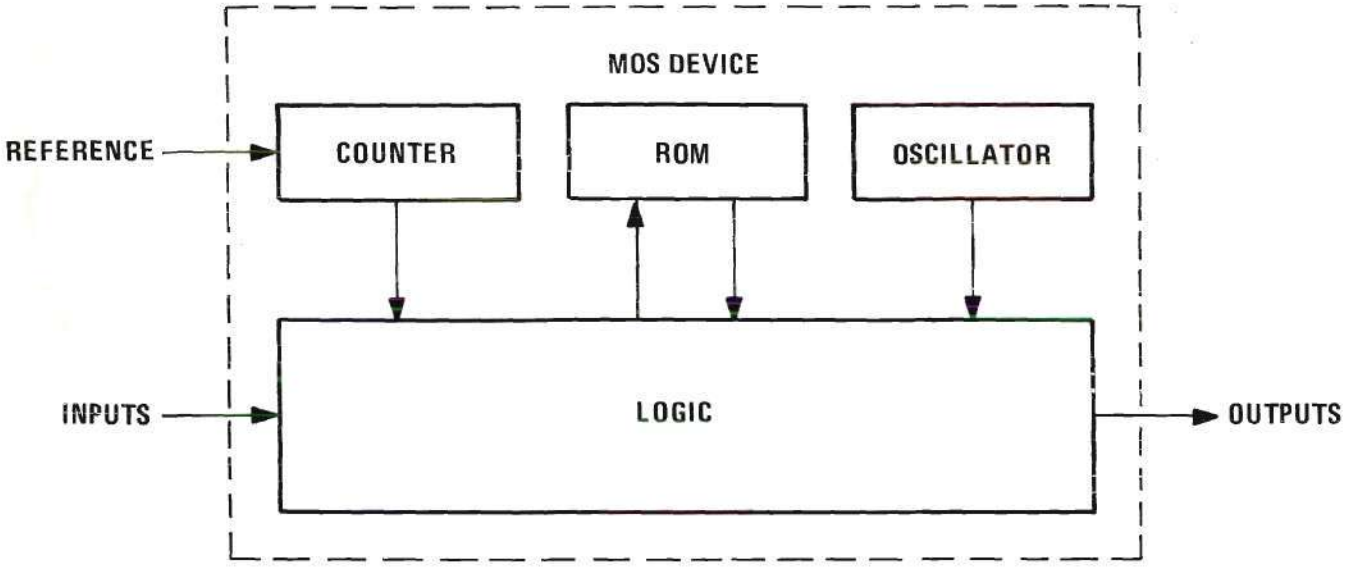


Figure 2. MOS Device Block Diagram

shows a block diagram of the MOS device. The purpose of each part of the MOS device is as follows:

(1) The counter is the basis of all function duration timing in the device. Using an external reference frequency, the counter determines how long a function lasts and therefore, when to change to another function. An example would be the timing of a two-minute agitation, followed by a one-minute drain, followed by a four-minute spin, and so on. The reference frequency used in the washer is the 60 hertz line frequency and the size of the counter permits real time durations of from a second up to around ten hours.

(2) The internal oscillator runs at about 75 kilohertz and provides a timing reference for obtaining information from the external input switches and for internal logical operations. The input to the MOS device is coded onto four time-shared multiplexed input lines. When the device needs input information, the switches are strobed by this oscillator signal.

(3) The read only memory is for the storage of states which are needed in certain logical operations.

(4) The remaining logic, which is a large portion of the MOS device, consists of gates and flip-flops which make decisions and perform the logical operations to step the washer through the proper functions for a particular cycle. This logic is dependent on the other three parts of the device

as well as on the external input switches for information concerning timing and function changes.

The external input switches are multiposition switches which select a cycle. These switches tie one of seven strobe lines to any combination of the four input lines. The switches include a cycle switch, a preparatory cycle switch, and several independent switches which can alter a portion of the cycle selected and can determine when the washer is full of water and off balance. As mentioned before, the MOS device strobes these switches to make its decisions on what functions to perform. The strobe signal itself is actually a rapidly changing impedance level which sinks current just as the outputs do, as explained in the next paragraph.

The purpose of the external driver circuits is to turn on and off the valves, solenoids, and indicator lamps according to the MOS device outputs. The MOS device has eighteen outputs which control all functions of the washer. Each output is similar to an open collector of a transistor with its emitter to ground. When the output is "on," meaning an element such as a solenoid should be energized, the output goes to ground while the "off" state is represented by a high impedance to ground. Since these transistors on the outputs are low current devices, an external driver transistor is used with each output. This driver transistor supplies current to the gate of a triac which switches current to the solenoid

or other element. Triacs are used as switches because all of the washer elements are 110 volt AC elements. Figure 3 shows how the MOS device is connected to typical input and output external circuitry.

Although the input-output relationships and the general layout of the MOS device are known, the actual logic and circuit design are not available. This fact limited the possible testing procedures as will be shown.

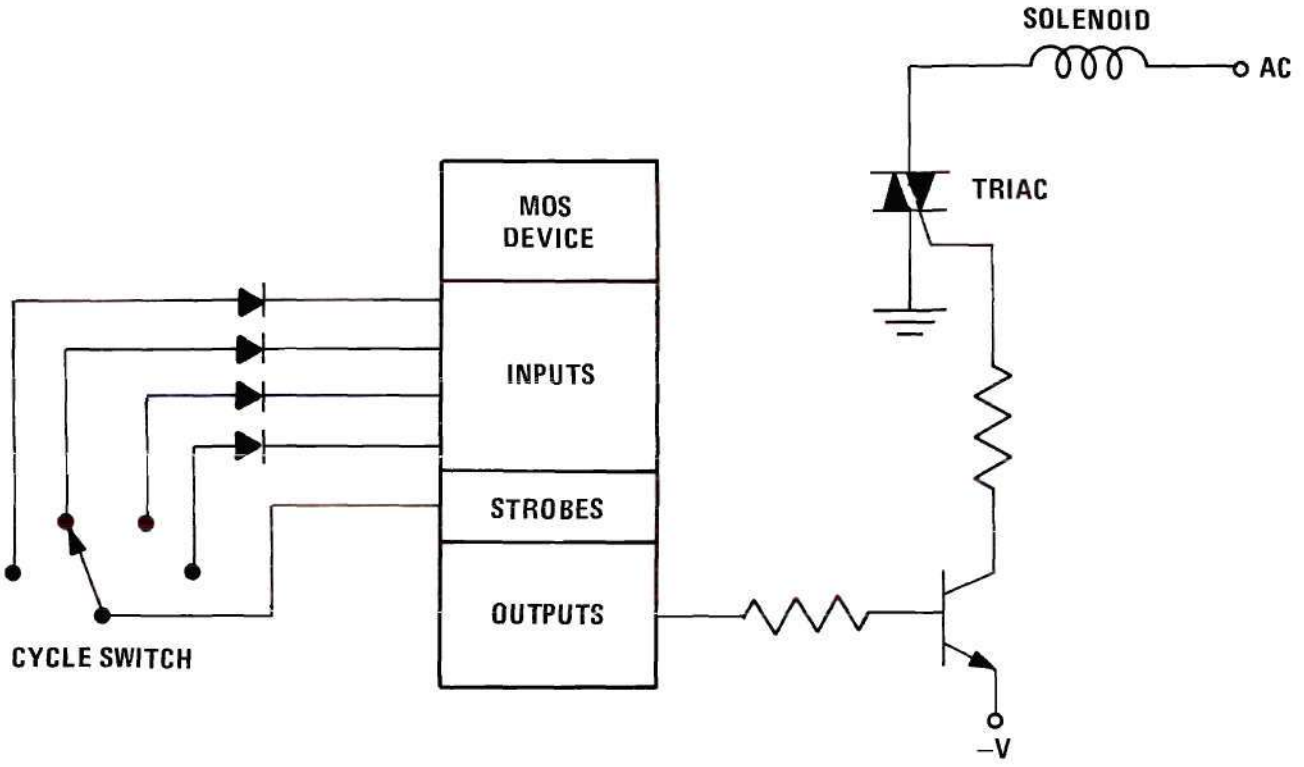


Figure 3. Typical Input and Output Circuitry

CHAPTER II

SYSTEM DESIGN AND CONSTRUCTION

General Considerations

The computer used to control the testing of the MOS integrated circuit is the NOVA 1200. The NOVA is a small general purposes computer requiring a basic interface to control an external device. Besides the MOS device to be tested, the NOVA is connected to several other input-output devices including a Teletype with paper tape reader and punch, a CRT display with keyboard, a line printer, and a magnetic tape unit. The interfacing for each external device is similar and so servicing the testing fixture for the MOS device is like servicing the Teletype or any other device. A block diagram of the computer with external devices is given in Figure 4.

As discussed in Chapter 1, the strobe for input information and the output information are both available as changing impedances with respect to ground. Since the computer and basic interface are five volt, transistor-transistor logic (TTL), these impedance changes must be translated to true, +5 volts, and false, 0 volts, logic levels for interpretation by the computer.

Concerning the overall test scheme, an attempt was made

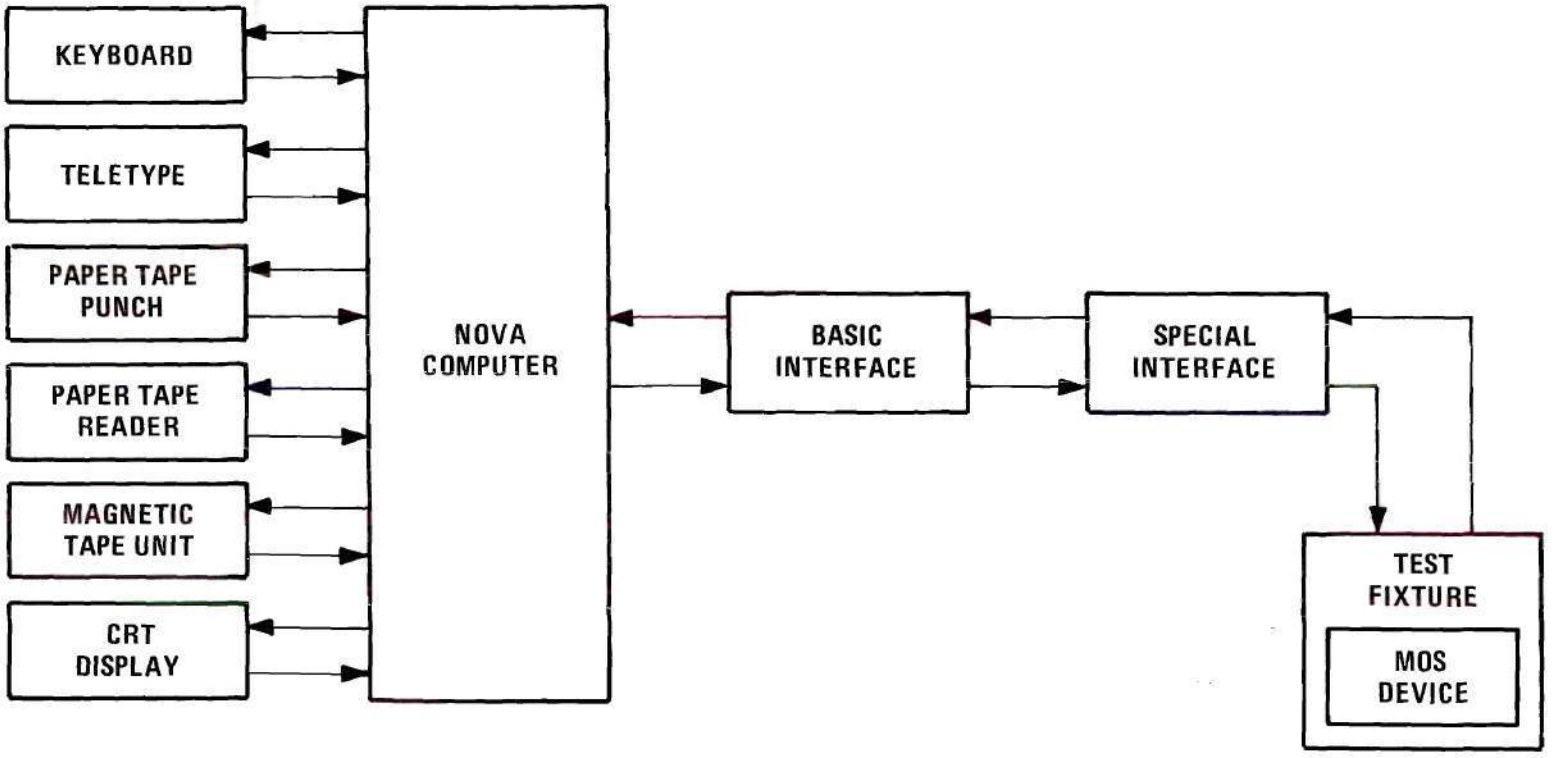


Figure 4. Computer With External Devices Block Diagram

to meet the following criteria:

(1) The test procedure should test the MOS device as thoroughly as possible, exercising a maximum number of the total gates and checking timing.

(2) The testing should take a minimum amount of time without reducing the test effectiveness.

(3) The test procedure should be flexible so that changes in the MOS device or in the requirements of the device can be incorporated into the testing.

The Basic Interface

The basic interface provides a means by which input and output data can be transferred between the computer and an external device. The interface allows the computer to select a particular device, control the flow of data to and from the computer and device, and hold the data for transfer at the proper time. These functions are performed in the interface by the following networks:

(1) The control network controls the flow of data in and out of the computer and device along a bi-directional sixteen-bit data bus. Using four flip-flops and other gates, the network tells the computer when the device is ready to accept or send out data. It specifies the state of the device, whether the device is busy or not, and requests interrupts so that data from the device can be put on the data bus.

(2) The device select network provides selection of a

particular external device using a six-bit octal code. When a device is to be serviced, its code is sent out on the data bus. Using inverters and a six-input AND gate, the network for the device recognizes its code and generates a signal to place three input and three output buffers on the data bus. This signal is anded with signals from the computer to specify which buffers should be on line for data transfer.

(3) Three input buffer networks and three output buffer networks hold data until the device is ready to accept or send out data. Each buffer holds sixteen bits of data using sixteen flip-flops. The buffers also contain an AND gate for each bit which ands the data with a signal specifying this device and a data-in or data-out command from the computer. The input buffers hold data from the computer until requested by the device.

A block diagram showing how the networks of the basic interface are interconnected with the computer, special interface, and MOS device is shown in Figure 5. Simplified logic diagrams of the basic interface networks are shown in Figures 6, 7, and 8. A more detailed description of the basic interface is given in the NOVA manual (12).

The basic interface was constructed on eight printed circuit cards which plug into a chassis. The eight cards include the control card, the device-select card, three input buffer cards, and three output buffer cards. The circuits

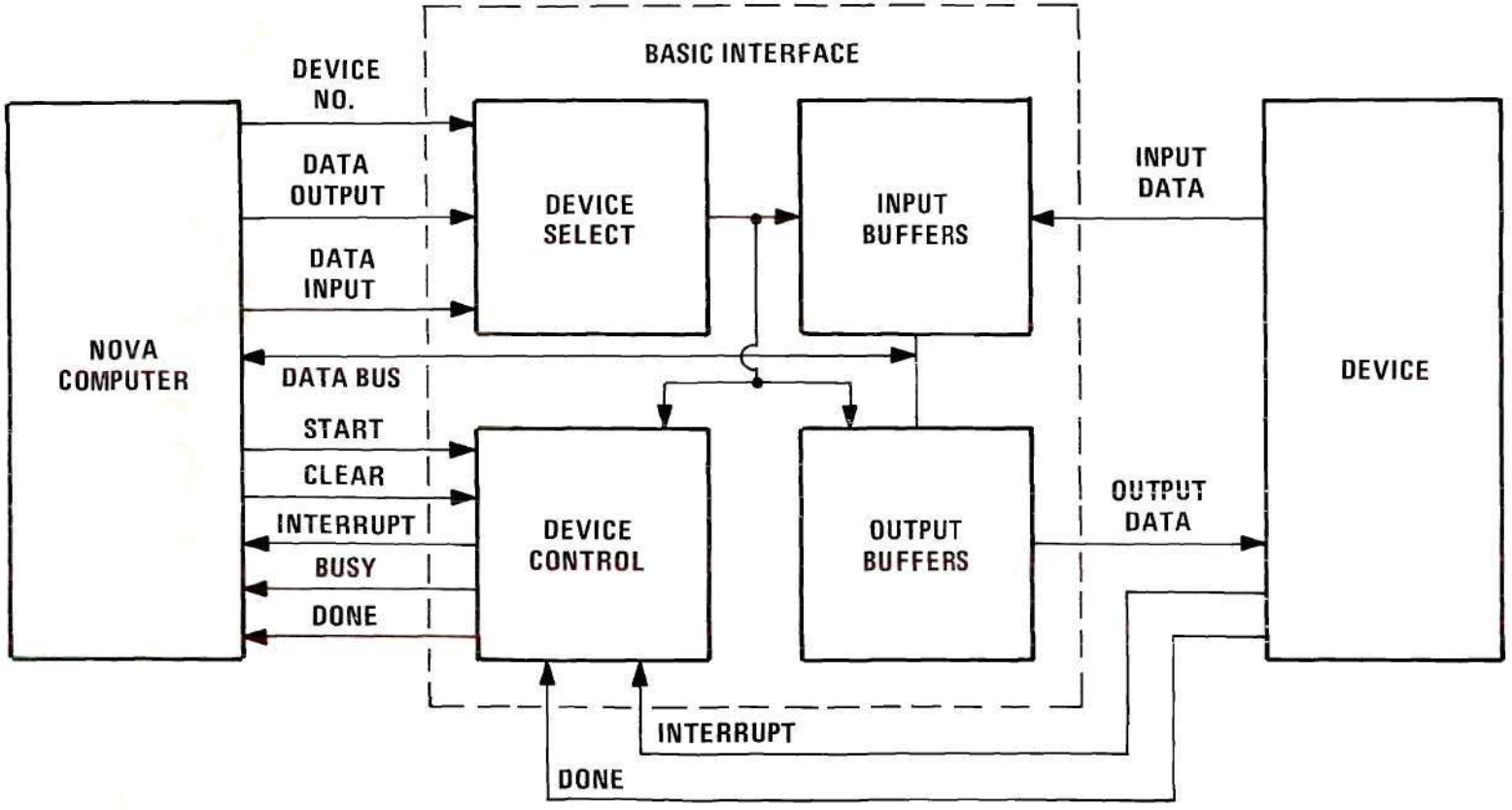


Figure 5. Basic Interface Block Diagram

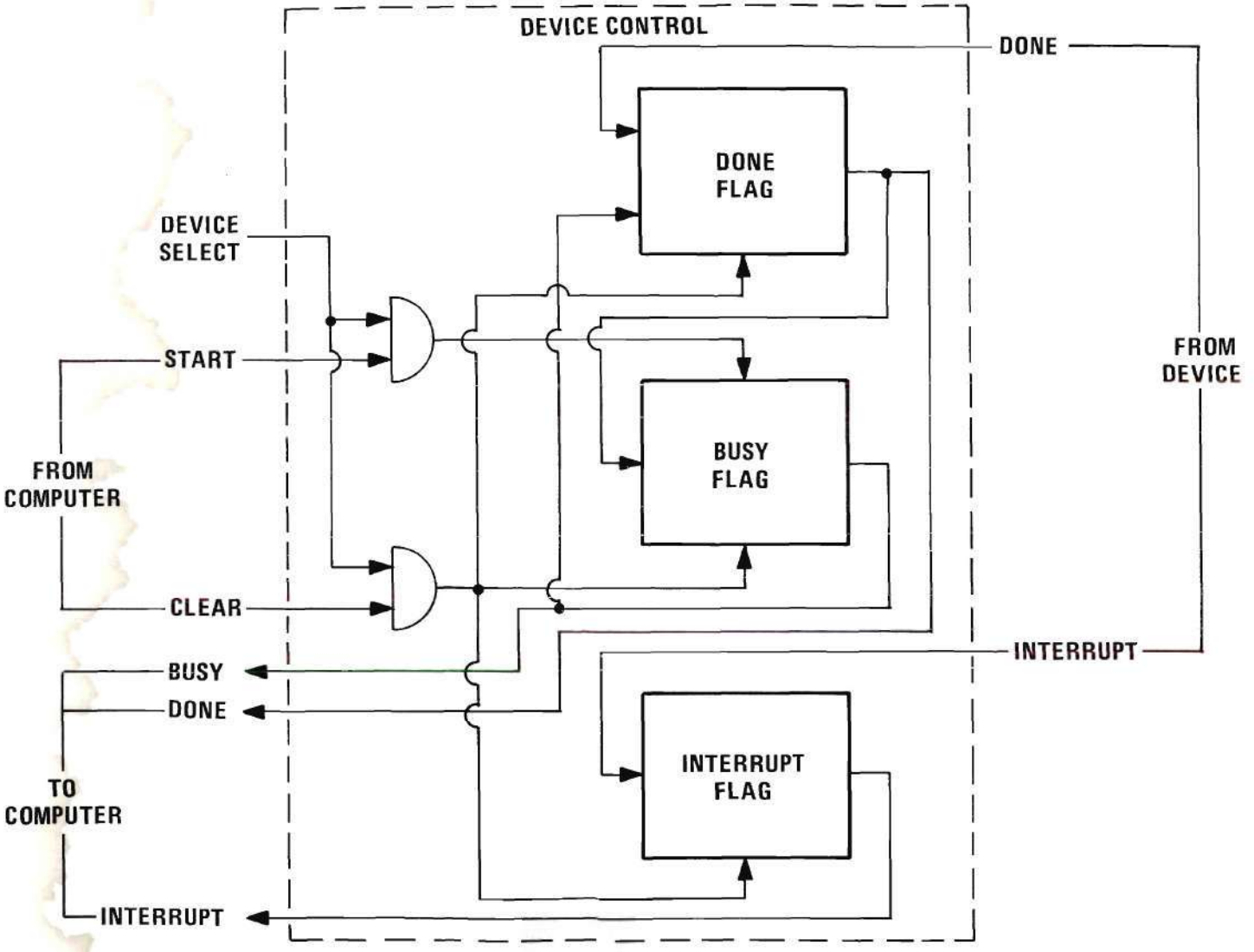


Figure 6. Simplified Device Control Network Logic Diagram

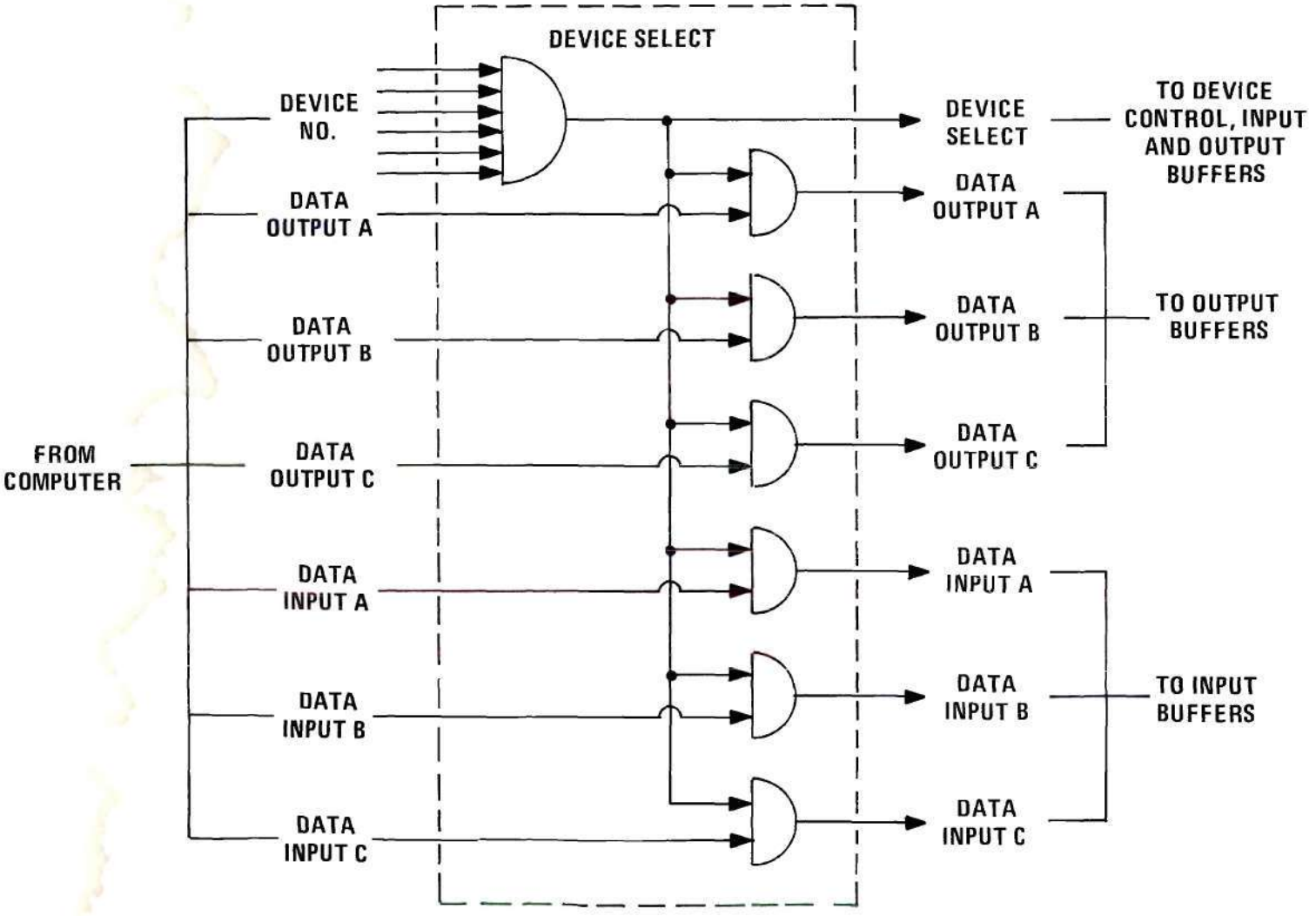


Figure 7. Simplified Device Select Network Logic Diagram

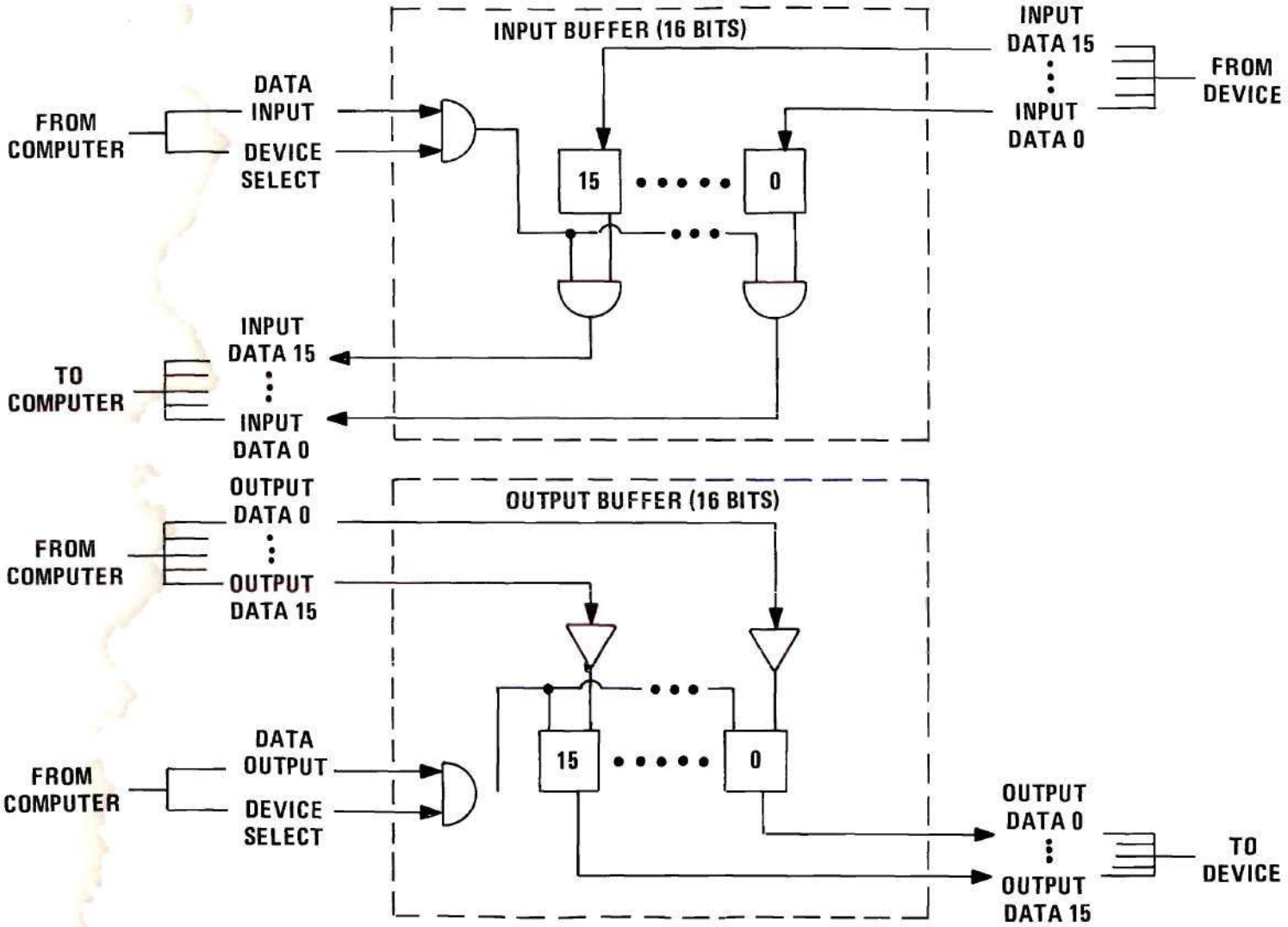


Figure 8. Simplified Input and Output Buffer Logic Diagrams

were built around TTL 7400 series integrated circuits. The circuits are powered by a five volt supply included in the chassis. The sixteen-bit data bus along with control lines are brought in and back out of the chassis through connectors. In all there are 50 lines from the computer which are common to all external devices. Therefore, the external devices, including the MOS device, are connected in a chain or in parallel. The chain is terminated in a resistor network as specified by the NOVA manual.

The Special Interface

In order to control and monitor the performance of the MOS device using the computer, a test fixture with special interfacing was designed and constructed. Recalling the test scheme criteria, a test fixture was needed which would make the outputs monitorable, the inputs programmable, and would permit testing at a maximum speed. To meet these requirements, interfacing was designed to include output level translators, input level translators, and a reference clock.

As described previously, the outputs of the MOS device determine which functions of the washer should be "on" and which functions should be "off." The "on" state is represented by a low impedance to ground, 1000 ohms or less, and the "off" state by a higher impedance to ground, 10,000 ohms or more. Also it is important to note that these impedance changes are evident only for a negative current to ground.

Therefore to translate these states to five volt logic levels, a two transistor circuit was used on each of the eighteen outputs. For a visual check and display purposes, a light emitting diode with driver was included on each output. The circuit diagram and an explanation is given in the appendix.

Since the input to the MOS device is simply a combination of switch closures between the strobes and the four input lines, the input level translators were designed to sink negative current, just as the strobes do, to represent the "on" or closed switch state. The circuit consists of three transistors for level translation and an AND gate by which the computer can select an input coding. The circuit diagram and the translated strobe signal are given in the appendix.

According to the MOS device manufacturer, the reference frequency should not exceed 2000 hertz due to synchronization problems between the reference frequency and the internal oscillator frequency. Therefore a crystal controlled clock was designed to run at this maximum frequency to make testing as fast as possible. A crystal was used for accuracy in determining how long a function lasts and for its low drift characteristics. As will be shown later, a counter in the computer program is set up to time each function. When a function change occurs, the counter is checked against upper and lower limits which have been set up previously using the crystal reference. This is why a low drift frequency source

is needed. The circuit itself uses a 100 kilohertz crystal and a divide-by-ten and a divide-by-five integrated circuit to get the 2000 hertz signal. Again the schematic is shown in the appendix.

Besides the level translators and clock, the special interfacing includes a power supply for the MOS device and a simple preset circuit which makes the device come on in the correct state. The MOS device supply is -25 volts which is also used as Vcc on the first stage of the level translators. The AND gates and other stages of the translators are powered by the basic interface supply of +5 volts. A block diagram of the complete special interface is shown in Figure 9.

The special interfacing circuitry was constructed on a wire-wrap plane of 14-pin, dual-in-line integrated circuit sockets. The input and output lines for the MOS device were brought out on a connector which plugs into the basic interface chassis.

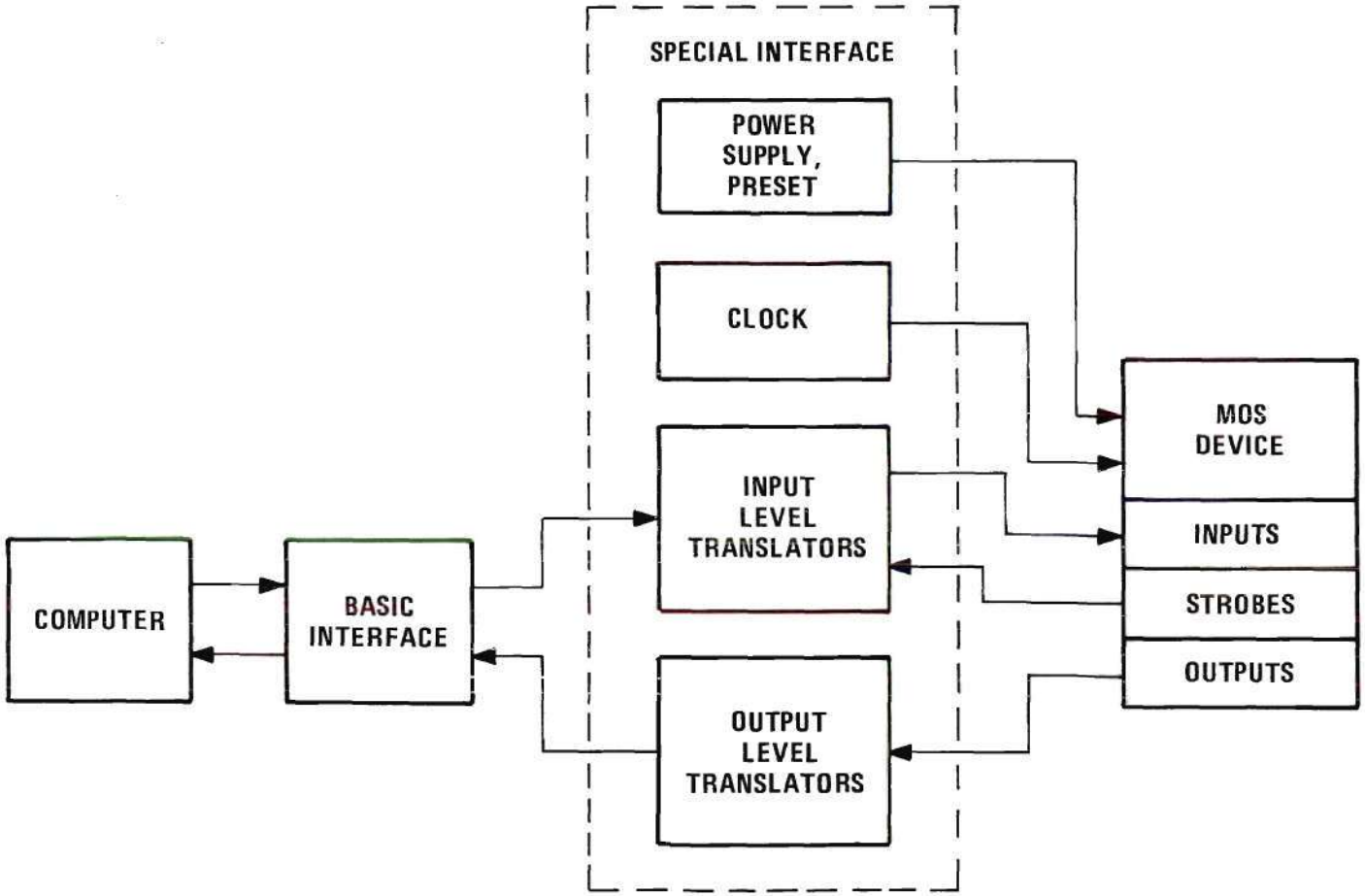


Figure 9. Special Interface Block Diagram

CHAPTER III

SYSTEM EVALUATION

Software Design

The function of the MOS device within the automatic washer dictates the requirements of a test procedure. The MOS device is supposed to take an input and step through the proper functions for that input at the proper times. Therefore a test procedure was designed to check the status of the device, or check which functions are "on," and to check the time duration of each status.

From the above requirements, a flow chart, shown in Figure 10, was made to describe the steps of the computer in testing the MOS device. The terms on the flow chart are defined as follows:

(1) The cycle is determined by a particular input coding which steps the device and washer through certain functions. For example, if the "delicate" cycle were selected, the washer would fill with warm water, agitate at medium speed, add detergent, add bleach, drain, spin spray, and so on. The input codings for the cycles are stored in a buffer in the computer and numbered consecutively, hence the cycle number.

(2) The status is the state of the MOS device outputs, either "on" or "off."

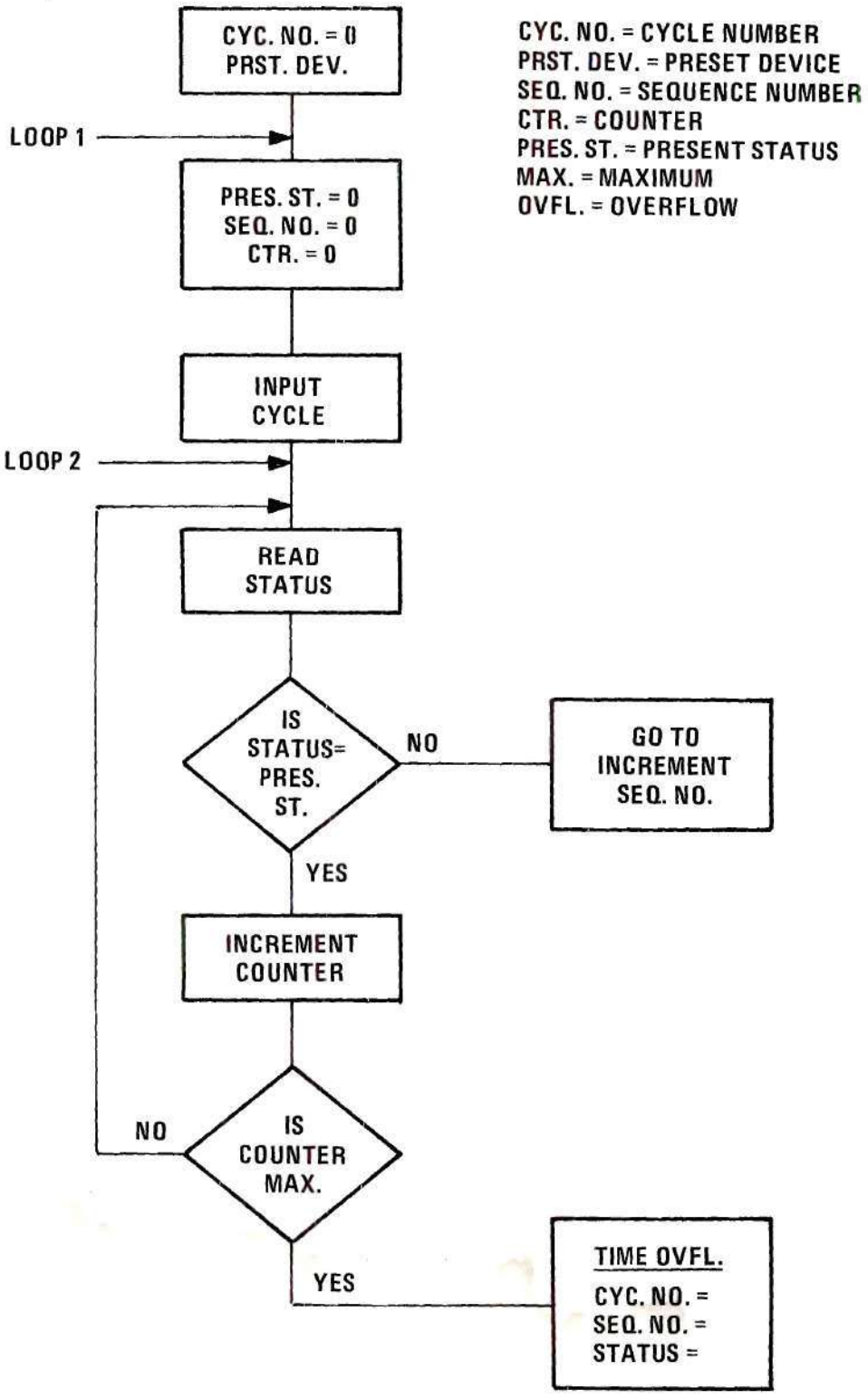


Figure 10. Computer Program Flow Chart (continued on following page)

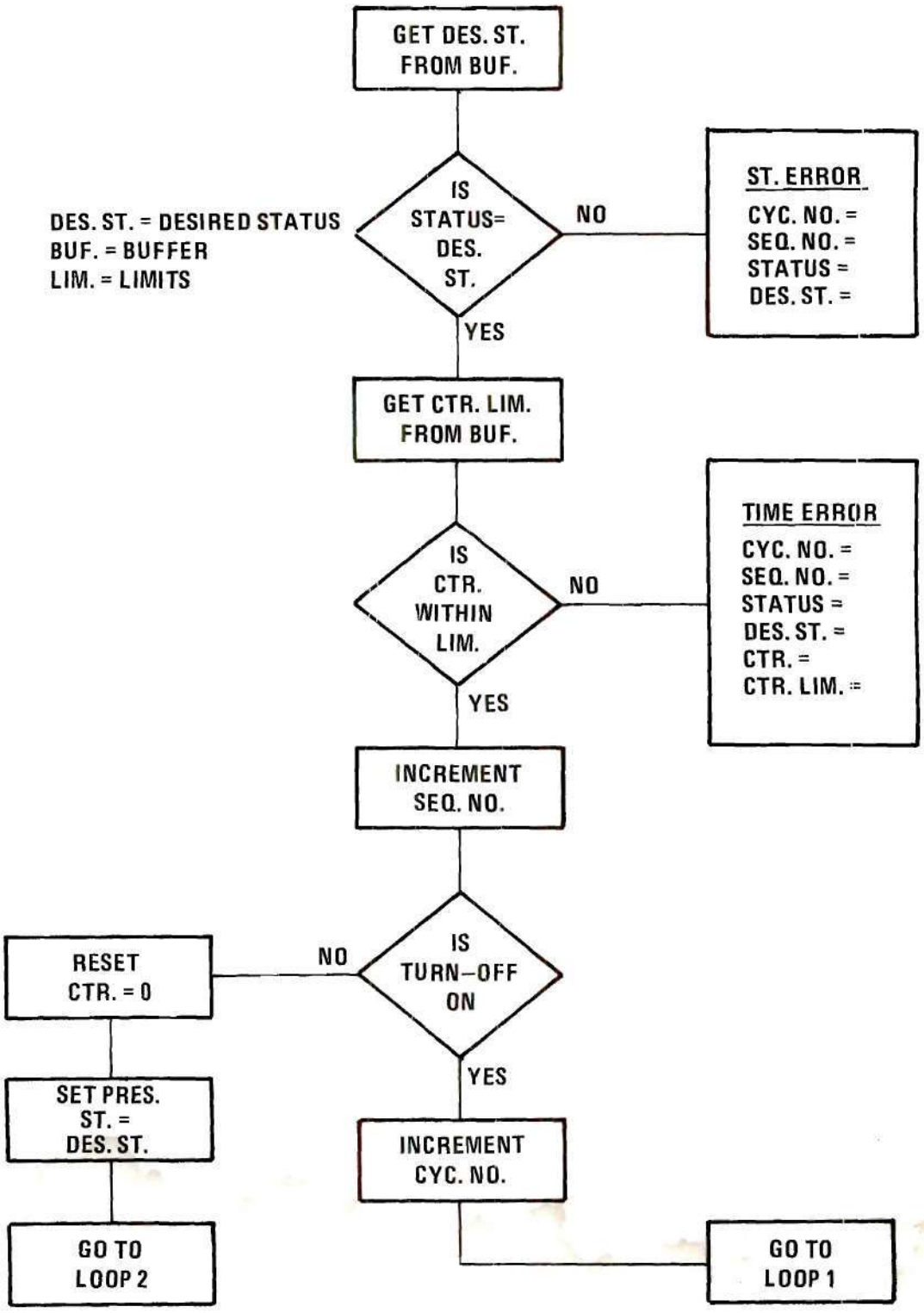


Figure 10. Computer Program Flow Chart

(3) The counter determines how long each status lasts. The counter is incremented in a program loop which takes the computer about 25 microseconds to execute.

(4) The present status is the output state just before the counter is incremented. The present status is used to determine if a status change has occurred.

(5) The desired status is the desired output state at a particular time.

(6) The sequence number keeps a record of how many different stati the MOS device has gone through. For example, sequence number one of the "delicate" cycle would be filling with warm water in which case the hot and cold water valves would be "on" and all other outputs "off."

(7) The counter limits give a maximum and a minimum time for the duration of each status or function.

(8) Turn-Off is the last output to come "on" in each cycle and therefore specifies the end of a cycle.

The following steps describe basically how the program works:

(1) The program is initialized by setting the present status and the incremented quantities to zero.

(2) A cycle is input to the MOS device. The cycle codings are stored in the input cycle buffer.

(3) The status of the device is read and if no status change has occurred, the counter is incremented. Each time the counter is incremented, the count is checked against a

maximum which is slightly greater than the count for the longest time duration of any status. If the count is greater than the maximum a time overflow error is output.

(4) If a status change has occurred, the new status is checked against the desired status which is stored in the desired status buffer. If the new status is incorrect, a status error is output.

(5) If the new status is correct, the time duration of the previous status is checked against upper and lower limits which again are stored in buffers.

(6) If the time duration is out of limits, a time error is output.

(7) If the time duration is within limits, the sequence number is incremented and the new status is checked for the turn-off state.

(8) If the turn-off is not "on," then this is the end of a sequence but not the end of the cycle and the counter is reset to zero, the present status is set equal to the desired status, and the status is read again.

(9) If the turn-off is "on," then this is the end of a cycle and the cycle number is incremented and the program goes back to the initialization of all quantities except the cycle number.

The complete computer program for the NOVA including the input cycle buffer, the desired status buffer, and the counter limits buffer for three cycles, is given in the appendix.

The desired status and counter limits buffers were generated using a good MOS device by putting in all zeroes initially and then replacing the zeroes with the desired data each time an error was output. For example, the first cycle chosen was the "Heavy Fabric" cycle. With all zeroes in the desired status buffer, a status error was output immediately upon starting the device. Since the error message includes the status when the error occurred, this status is put in as the first entry in the buffer. Then the program and device are restarted and naturally a time error occurs because the first status lasts longer than zero counts which is the upper limit. Again the time error message tells the correct count, upper and lower limits are selected and put into the buffer, and the process starts over. The time limits are selected according to the device requirements (13) which gives the timing accuracy as $\pm$10% or $\pm$10 minutes whichever is less. Whenever an error occurs, the program is set up to print out the error on the Teletype or line printer and then go to "Debug" which is a canned NOVA program providing direct access to the core memory locations and to the accumulators.

A Sample Test

The sample test to be described consists of generating the desired data buffers for three cycles and of simulating errors within these cycles to demonstrate the error detection and output. With three cycles, all of the program's routines

are demonstrated including the test for turn-off, the incrementing of the cycle number, and the incrementing of the desired data buffer addresses.

The three cycles tested were the "Heavy Fabric," followed by "Short Wash" with "Prewash" and "Cold Water Only," followed by "Sanitize." These were chosen because the "Heavy Fabric" is fairly long and includes most of the washer functions, "Short Wash" with "Prewash" and "Cold Water Only," demonstrates the use of the preparatory cycle with an independent control, and "Sanitize" is a short cycle but helps to demonstrate the transition from one cycle to another. Figure 11 shows a flow chart of the washer's operation with the paths marked according to the possible cycle selections. The relationship between the cycle selection switches as they would appear on a washer is explained in more detail in the appendix.

Tables 1, 2, and 3 show the input coding for each cycle along with the status for each sequence or function through which the MOS device is stepped. By comparing the flow chart with the sequences on the table, it can be seen that there are many more status changes than is obvious from the flow chart. For example, the "Heavy Fabric" cycle included 48 sequences or status changes while on the flow chart there are 25 blocks to indicate status changes. The difference lies in the fact that although several functions or outputs appear to come on at the same time, they come on one at a time and the computer, with its 25 microseconds loop time, can recognize these fast

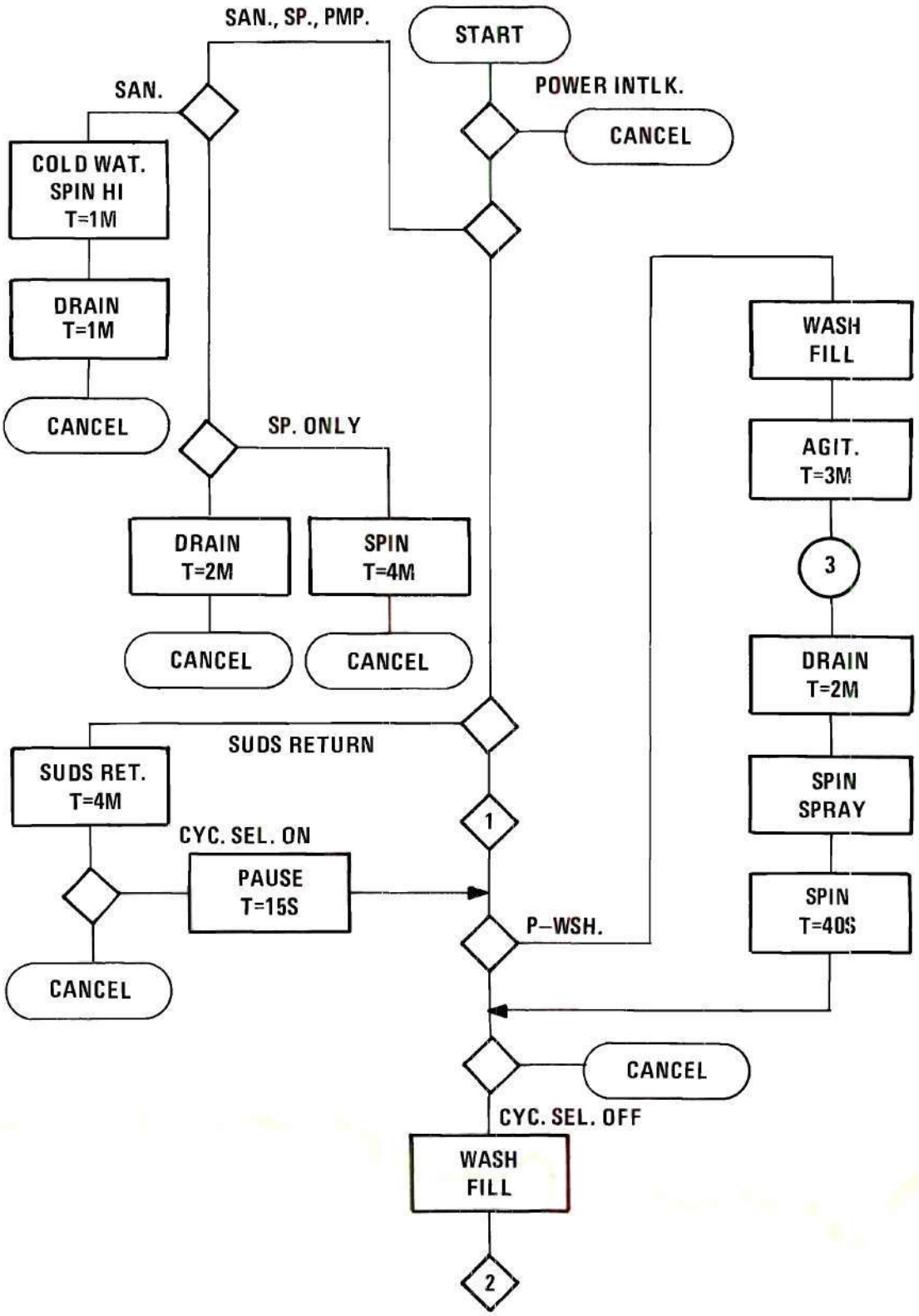


Figure 11. Washer Operation Flow Chart (continued on following pages)

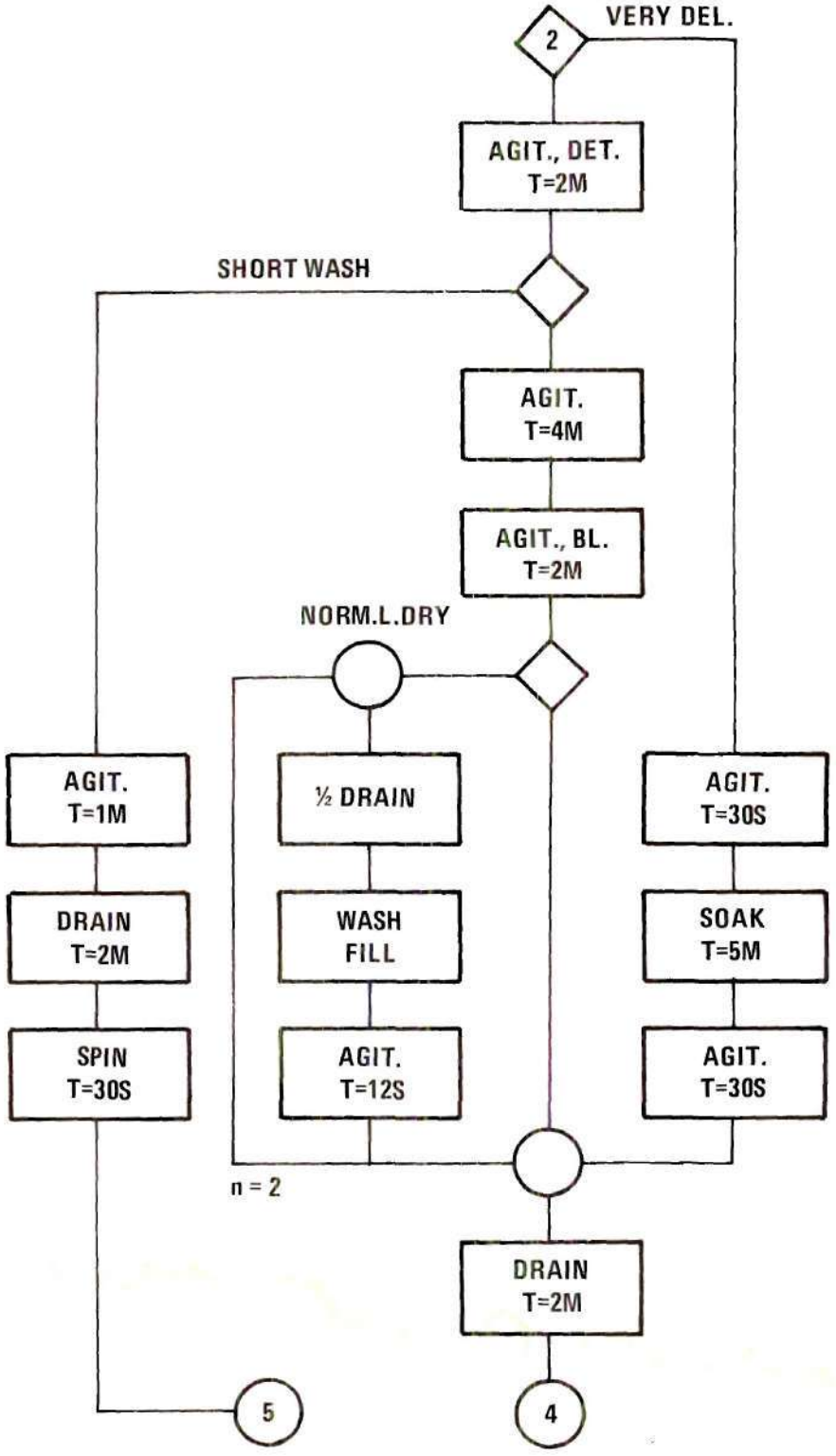


Figure 11. Washer Operation Flow Chart

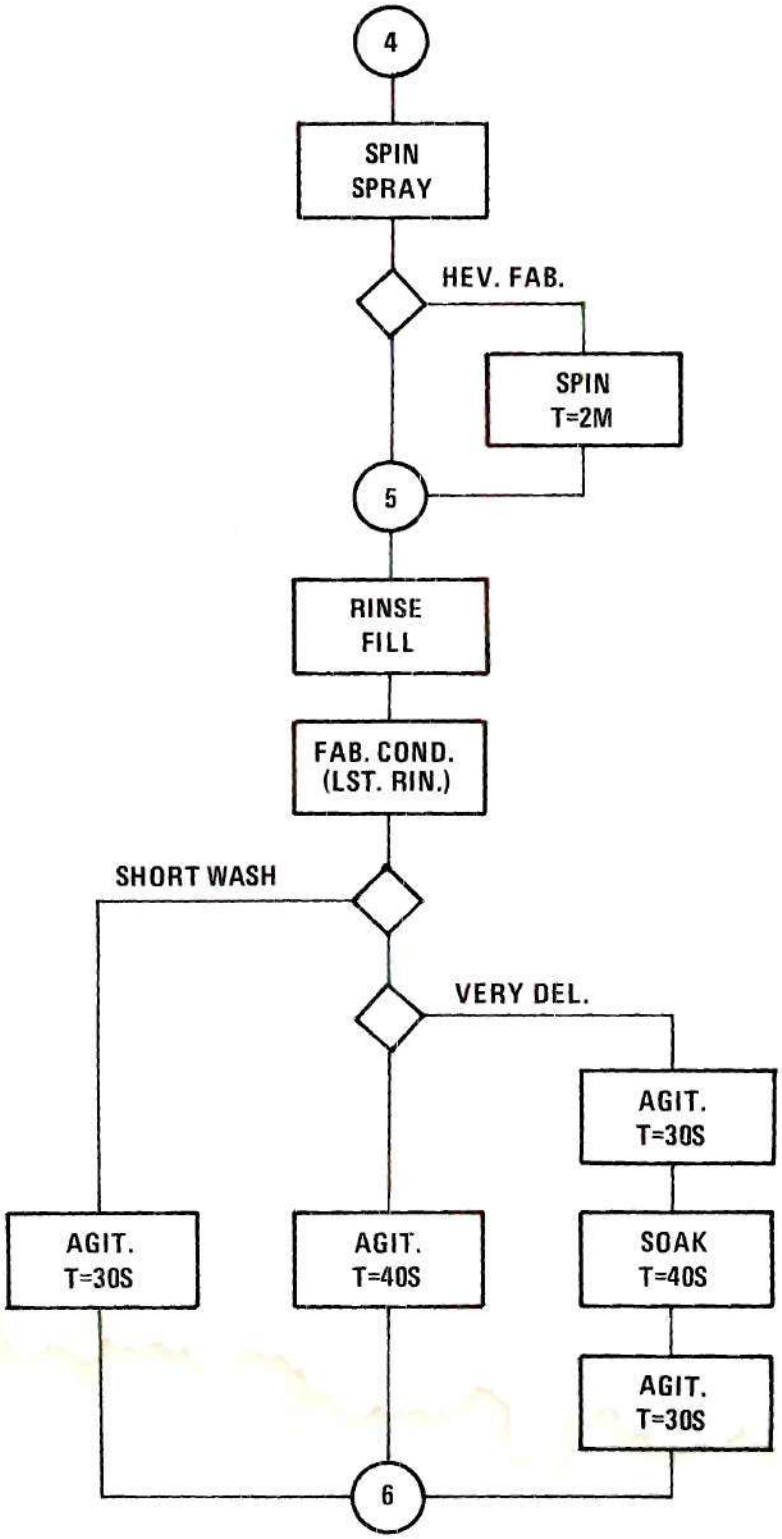


Figure 11. Washer Operation Flow Chart

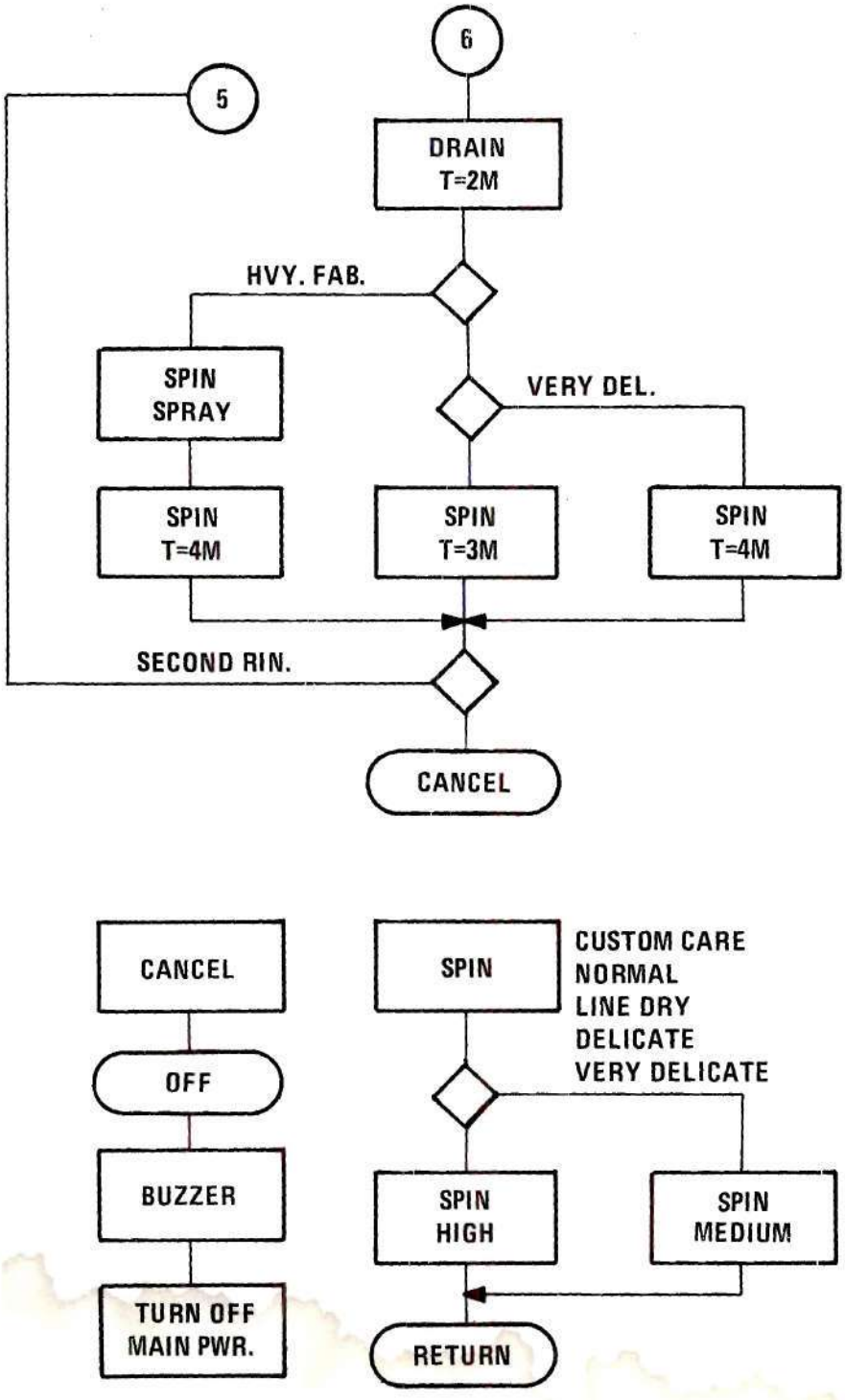


Figure 11. Washer Operation Flow Chart

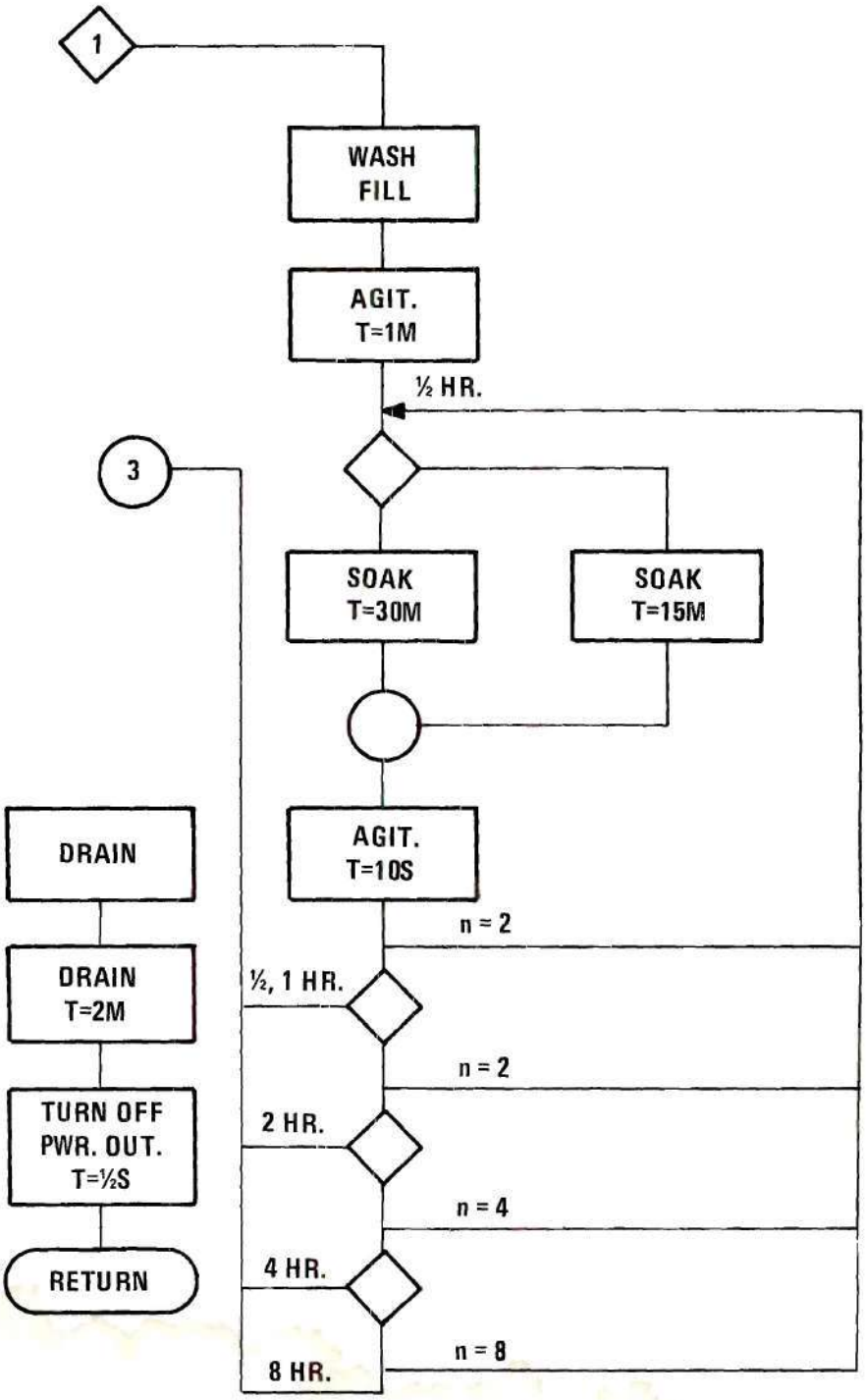


Figure 11. Washer Operation Flow Chart

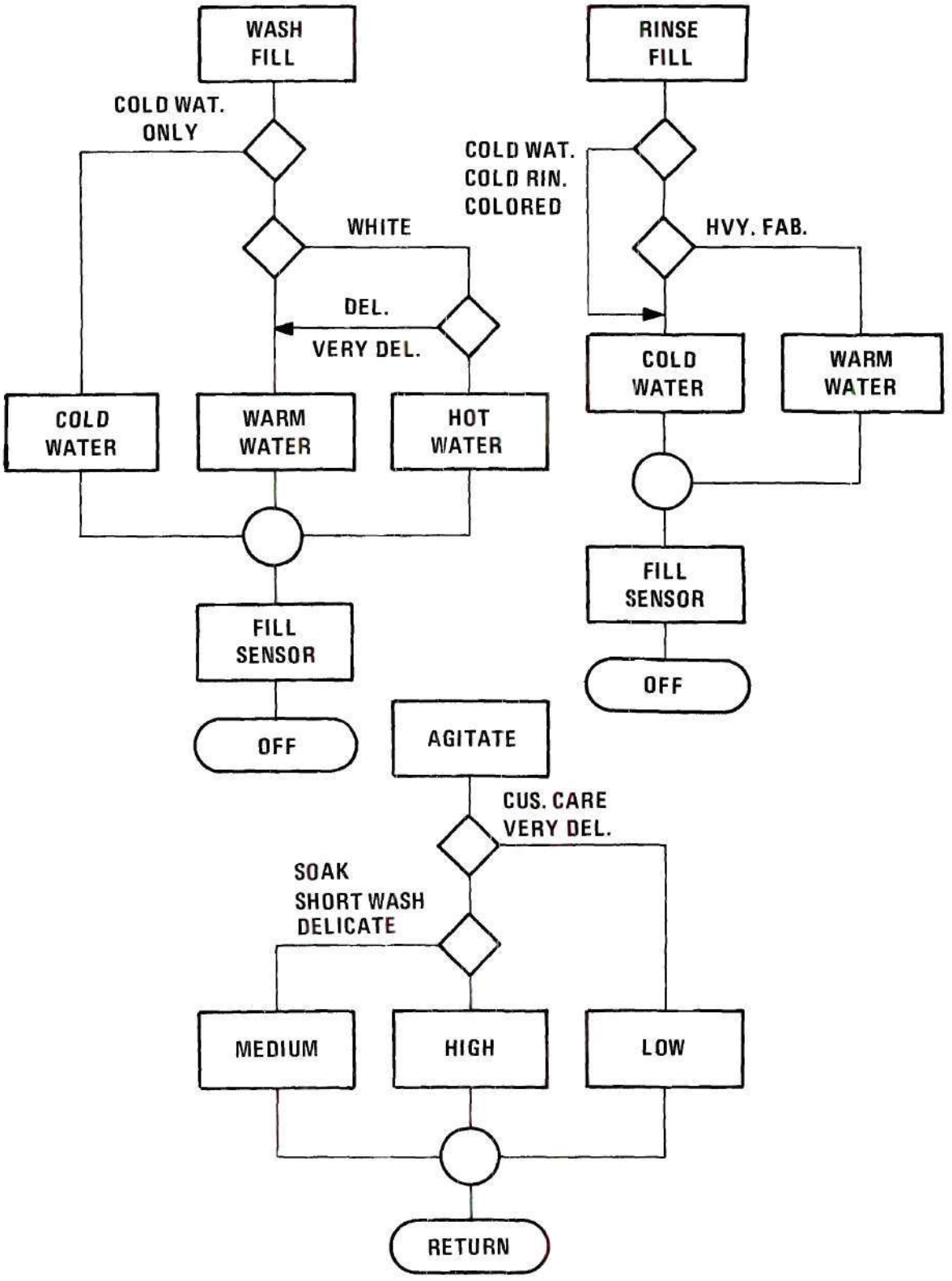


Figure 11. Washer Operation Flow Chart

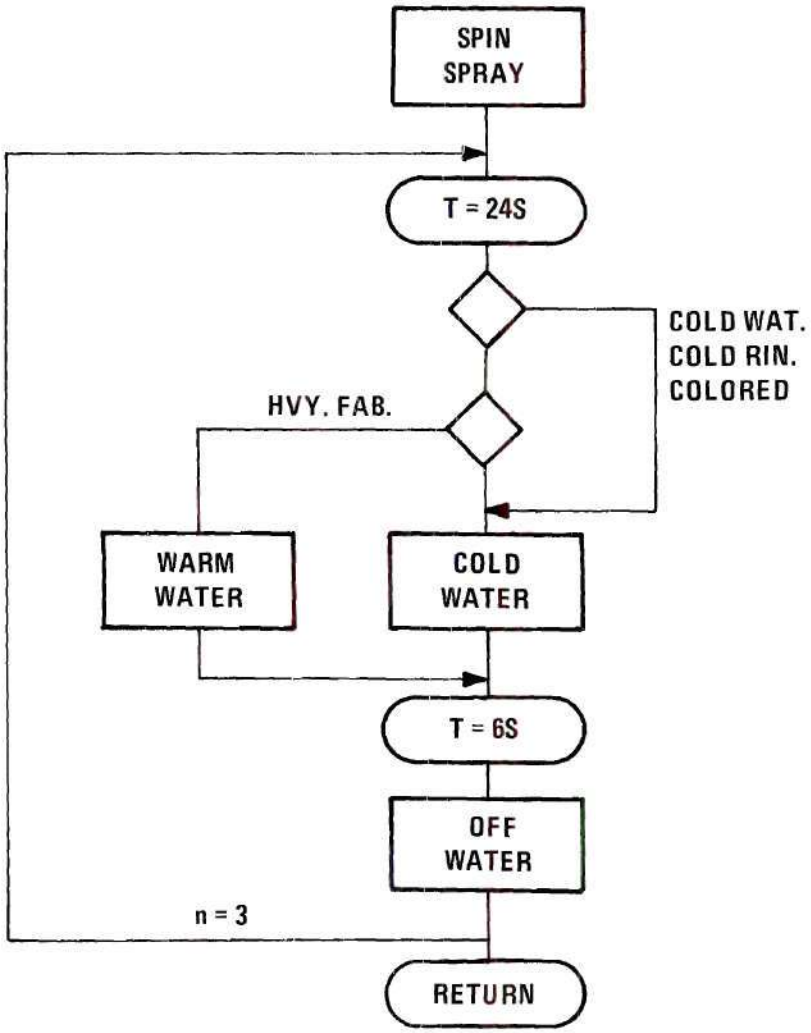


Figure 11. Washer Operation Flow Chart

Abbreviations on Flow Chart

Agit.=Agitate

Bl.=Bleach

Cond.=Conditioner

Cus.=Custom

Cyc.=Cycle

Del.=Delicate

Fab.=Fabric

Hi=High

Hr.=Hour

Hvy.=Heavy

Intlk.=Interlock

L.Dry=Line Dry

Lst.=Last

M=Minute

Norm.=Normal

Out.=Output

Pmp.=Pump

Pwr.=Power

P-Wsh=Prewash

Ret.=Return

Rin.=Rinse

S.=Second

San.=Sanitize

Sel.=Select

Sp.=Spin

T=Time

Wat.=Water

Note: The circles and diamonds enclosing numbers on the flow chart designate points where the flow chart continues on another page.

Figure 11. Washer Operation Flow Chart (concluded)

Table 1. Cycle 0 Output Sequences

Input = Start, Full, Heavy Fabric

Sequence Number

Outputs	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Prewash Lamp																						
Soak Lamp																						
Wash Lamp	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Rinse Lamp																						
2nd Rinse Lamp																						
Agitate				X	X	X	X	X														
Spin																		X	X	X	X	X
Motor Low									X						X							
Motor Medium																						
Motor High				X	X	X	X						X					X	X	X	X	X
Detergent					X																	
Bleach							X	X	X	X												
Fabric Cond.																						
Suds Return												X	X	X	X	X						
Cold Water		X																	X		X	
Hot Water		X																	X		X	
Buzzer																						
Turn-Off																						

Note: An X indicates that the output is "on" for the corresponding sequence.

Table 1. Continued

Sequence Number

Outputs	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
Prewash Lamp																						
Soak Lamp																						
Wash Lamp	X	X	X																			
Rinse Lamp				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd Rinse Lamp																						
Agitate							X	X														
Spin	X	X															X	X	X	X	X	X
Motor Low										X					X							
Motor Medium																						
Motor High	X	X					X	X					X				X	X	X	X	X	X
Detergent								X	X	X	X											
Bleach																						
Fabric Cond.								X	X	X	X											
Suds Return																						
Cold Water	X				X													X		X		X
Hot Water	X				X													X		X		X
Buzzer																						
Turn-Off																						

Table 1. Continued

Sequence Number

Outputs	44	45	46	47
Prewash Lamp				
Soak Lamp				
Wash Lamp				
Rinse Lamp	X	X	X	X
2nd Rinse Lamp				
Agitate				
Spin	X			
Motor Low				
Motor Medium				
Motor High	X			
Detergent				
Bleach				
Fabric Cond.				
Suds Return				
Cold Water				
Hot Water				
Buzzer			X	
Turn-Off				X

Table 2. Cycle 1 Output Sequences

Input = Start, Full, Prewash, Cold Water Only

Sequence Number

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Outputs	Prewash Lamp	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
	Soak Lamp																						
	Wash Lamp																				X	X	X
	Rinse Lamp																						
	2nd Rinse Lamp																						
	Agitate				X																		
	Spin												X	X	X	X	X	X	X				
	Motor Low						X				X												
	Motor Medium																						
	Motor High				X				X				X	X	X	X	X	X	X				
	Detergent																						
	Bleach																						
	Fabric Cond.																						
	Suds Return																						
	Cold Water		X											X		X		X					
	Hot Water																						
	Buzzer																						
	Turn-Off																						

Table 2. Continued

Outputs	Sequence Number																					
	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
Prewash Lamp																						
Soak Lamp																						
Wash Lamp	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Rinse Lamp																						
2nd Rinse Lamp																						
Agitate	X	X	X	X																		
Spin															X	X	X	X	X	X	X	
Motor Low						X						X										
Motor Medium																						
Motor High	X	X	X	X						X					X	X	X	X	X	X	X	
Detergent		X																				
Bleach				X	X	X	X															
Fabric Cond.																						
Suds Return									X	X	X	X	X									
Cold Water																X		X		X		
Hot Water																						
Buzzer																						
Turn-Off																						

Table 2. Continued

	Sequence Number																
	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
Outputs																	
Prewash Lamp																	
Soak Lamp																	
Wash Lamp																	
Rinse Lamp	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2nd Rinse Lamp																	
Agitate				X	X												
Spin														X			
Motor Low							X					X					
Motor Medium																	
Motor High				X	X					X				X			
Detergent					X	X	X	X									
Bleach																	
Fabric Cond.					X	X	X	X									
Suds Return																	
Cold Water		X															
Hot Water																	
Buzzer																X	
Turn-Off																	X

Table 3. Cycle 2 Output Sequences

Input = Start, Full, Sanitize

Sequence Number

Outputs	0	1	2	3	4	5	6	7	8	9
Prewash Lamp										
Soak Lamp										
Wash Lamp										
Rinse Lamp										
2nd Rinse Lamp										
Agitate										
Spin		X								
Motor Low				X						
Motor Medium										
Motor High		X					X			
Detergent										
Bleach										
Fabric Cond.										
Suds Return										
Cold Water	X	X	X	X	X					
Hot Water										
Buzzer									X	
Turn-Off										X

transitions. For example, in the first part of the "Heavy Fabric" cycle even though the input tells the device that the washer is full of water, the hot and cold water outputs come on for an instant before the device goes to wash. When it does go to wash, first the wash indicator comes on, then the agitate and motor medium come on, and finally the detergent comes on. Therefore the device goes through five stati whereas the flow chart indicates two.

To demonstrate the status error detection, two switches were put in to break output lines. One breaks the bleach output line and the other breaks the cold water output line. Figure 12 illustrates the status error messages output when the bleach line was broken during the "Heavy Fabric" cycle and when the cold water line was broken before spin spray of the "Short Wash" cycle and before the beginning of the "Sanitize" cycle. The status error messages are programmed to print out the cycle number and sequence number in decimal, and the status and desired status in binary. The status and desired status indicate the states of the 18 outputs, "1" for "on" and "0" for "off." In the error message the right most position is Output 1 with the positions numbered consecutively going to the left up to Output 18. The functions of the 18 outputs are as follows:

(1) Prewash Lamp

(2) Soak Lamp

(3) Wash Lamp

```
*STATUS ERROR
CYCLE NO.=.........+00000
SEQUENCE NO.=.......+00006
STATUS=.............0000000010001001OO
DESIRED STATUS=.....0000001010001001OO
```

Bleach Off During Heavy Fabric Cycle

```
*STATUS ERROR
CYCLE NO.=.........+00001
SEQUENCE NO.=.......+00037
STATUS=.............0000000010010001OO
DESIRED STATUS=.....0001000010010001OO
```

Cold Water Off Before Spin Spray of Short Wash Cycle

```
*STATUS ERROR
CYCLE NO.=.........+00002
SEQUENCE NO.=.......+00000
STATUS=.............0000000000000000OO
DESIRED STATUS=.....0001000000000000OO
```

Cold Water Off Before Beginning of Sanitize Cycle

Figure 12. Status Error Messages

(4) Rinse Lamp

(5) 2nd Rinse Lamp

(6) Agitate

(7) Spin

(8) Motor Low

(9) Motor Medium

(10) Motor High

(11) Detergent

(12) Bleach

(13) Fabric Conditioner

(14) Suds Return

(15) Cold Water

(16) Hot Water

(17) Buzzer

(18) Turn-Off

Typical time error and time overflow error messages are given in Figure 13. These were simulated by setting bad limits in the counter limits buffers. The time error messages print out the cycle number, sequence number, status, and desired status the same as in the status error message. In addition, the count of the counter and the upper and lower limits are printed out in octal. Because of the length of some of the functions, the counter and the limits must be represented by two six-bit octal words, hence the high and low designations.

```
*TIME ERROR
CYCLE NO.=.........+00000
SEQUENCE NO.=.......+00005
STATUS=.............000000001000100100
DESIRED STATUS=.....000000001000100100
HIGH UPPER LIMIT=....000001
LOW UPPER LIMIT=.....020000
HIGH COUNTER=........000001
LOW COUNTER=.........037521
HIGH LOWER LIMIT=....000001
LOW LOWER LIMIT=.....010000

Low Upper Limit Set Too Low
```

```
*TIME OVERFLOW ERROR
CYCLE NO.=.........+00000
SEQUENCE NO.=.......+00024
STATUS=.............0000000000000000100

High Counter Maximum Set Too Low
```

Figure 13. Typical Time and Time Overflow Error Messages

Conclusions

The results of the sample test proved the workability of the computer program and the interfacing. Since the interfacing is basic for the MOS device, the computer program is straight forward and easily modified. There are no synchronization problems between the computer and device. The error messages along with the "Debug" program make errors and inconsistencies in status and timing easy to locate.

In summary, this test system is effective and will detect a bad device. Likewise, the sample test pointed out the limitations of the system which will be discussed in the next chapter.

CHAPTER IV

LIMITATIONS

The test system as described in this thesis is rather limited in its direct application to large scale testing of the MOS device. The system is definitely thorough and accurate since it is designed to test every status of every cycle and time every status in 25 microsecond increments. However, the speed at which a number of devices can be tested with this system is very limited.

First, since the actual design of the MOS device is not available, it is assumed that every possible cycle should be tested from start to turn-off. Although some functions are common to several cycles, as can be seen on the flow chart of Figure 11, it is not known if the transition into and out of these functions are identical or even if the functions themselves are identical. Hence, every possible combination of the 10-position cycle switch, the 8-position preparatory cycle switch, and the nine independent switches must be tested. The number of possible different cycles comes out to about 4800.

The "Heavy Fabric" cycle, for example, takes about 25 minutes real time to complete. With 2000 hertz reference, the testing takes 45 seconds. A 45-second test is typical for a cycle with no preparatory cycle soak time. However,

real time soak times of 1/2, 1, 2, 4, and 8 hours are available which alone would take about 3/4, 1 1/2, 3, 6, and 12 minutes to test. Therefore, the total testing time for all cycles of even one device would be prohibitively large.

Secondly, the time required to generate the desired data buffers is also large, although this data is stored and has to be generated only once. With this test system, the only way to generate the desired data is to run the device as described in Chapter III, filling the buffers from the error messages. This method gives the correct status and time for each status change. The drawback is that after each status change and entry of the desired data, the device must be restarted and run out again to the next status change. Again using the "Heavy Fabric" cycle as an example, the filling of the buffers takes about four hours.

The sample test pointed out several other limitations which are not real problems but merely require computer program changes. One change was made when the sample test revealed that on going from one cycle to the next the MOS device should be stopped and restarted after a delay. Without the delay and restart, the status after the transition is arbitrary. The program was changed such that the preset voltage is turned off, the inputs to the MOS device are zeroed, and then, after a three second delay, the device is restarted at the next cycle. This also increased the testing time.

A similar situation exists when the MOS device is

preset at the beginning of any cycle. Since the computer execution time of a typical instruction is only 1.35 microseconds, the continuation of the computer program must be delayed to let the preset voltage come up before a cycle is input. Without this delay the first status is arbitrary. A delay of one second was put in after the preset voltage was turned on to remedy this problem. Again the testing time had to be lengthened.

Finally, it was noted that, upon switching off an output to simulate a status error, the status error message contained a status different from that expected. When an output is turned off one would expect the incorrect status printed out to be the desired status with the corresponding output off rather than on. However, if the output turned off is the only change from the previous status, then the computer does not see a status change and goes on to read the next status after the status in which the error actually occurred. It is still known that an error has occurred, but the exact cause is not obvious. Therefore to make the error detection more convenient, the program should be rearranged to check the status time duration before the status change rather than afterward, such that the computer would recognize the extended time duration of the previous correct status.

Obviously, the big limitations of the test system are in testing time. Several recommendations will be made in Chapter V to reduce this problem.

CHAPTER V

RECOMMENDATIONS

The limitations on the MOS device test system were shown to be entirely in the areas of test preparation time and real testing time. The following recommendations will be made to reduce these times to more practical lengths:

(1) If the device design and timing information were available, the desired data buffers would be known and would not have to be generated.

(2) If the above information were not known, the computer program could be extended to fill the buffers using a good device.

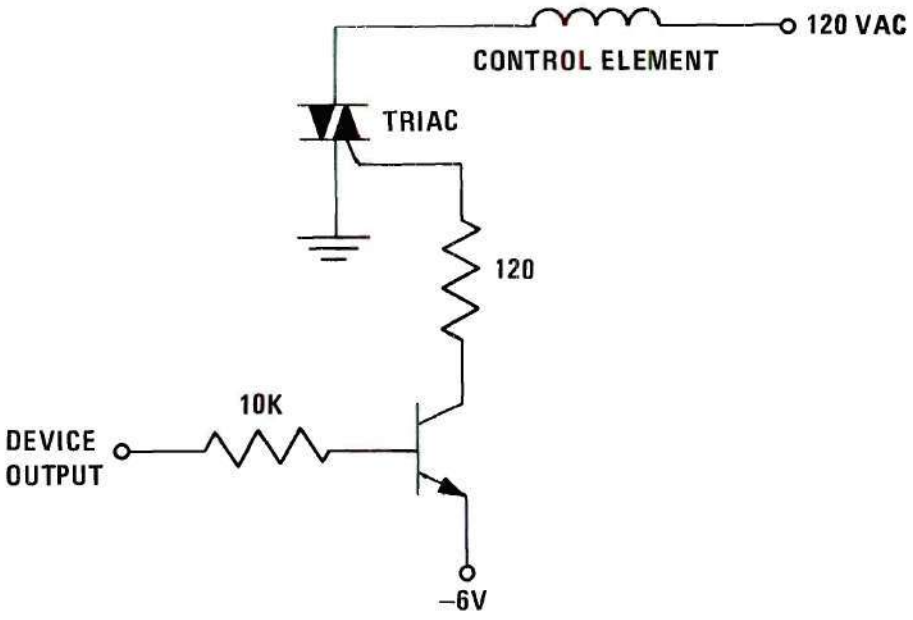
(3) The MOS device could be run synchronously using the internal oscillator's signal as the reference which is much higher in frequency.

(4) Again if the device design were available, the external test pins could be used to test each part of the device, the read only memory, counter, and logic, separately and in minimum time.

Since the real success in testing the MOS device, especially in large scale, depends so much on information from the manufacturer, either the manufacturer's test must be relied upon or that information must be made available.

APPENDIX A

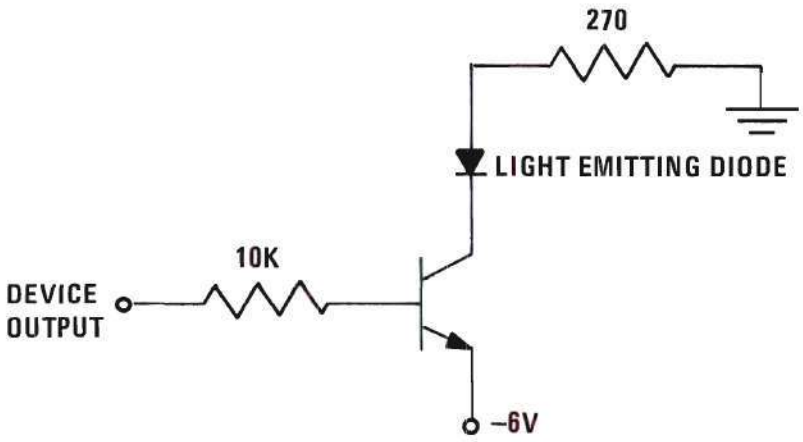
ELECTRONIC TIMER SCHEMATICS



Typical Washer Control Element Output Driver Schematic

Description: The above circuit is used on the 13 washer control elements which include solenoids, relays, the motor, and a buzzer. When the MOS device output is on or grounded, the transistor is forward biased. Current flows through the 120 ohm current limiting resistor into the gate of the triac to turn it on. AC current flows through the triac and the control element which produces some mechanical action.

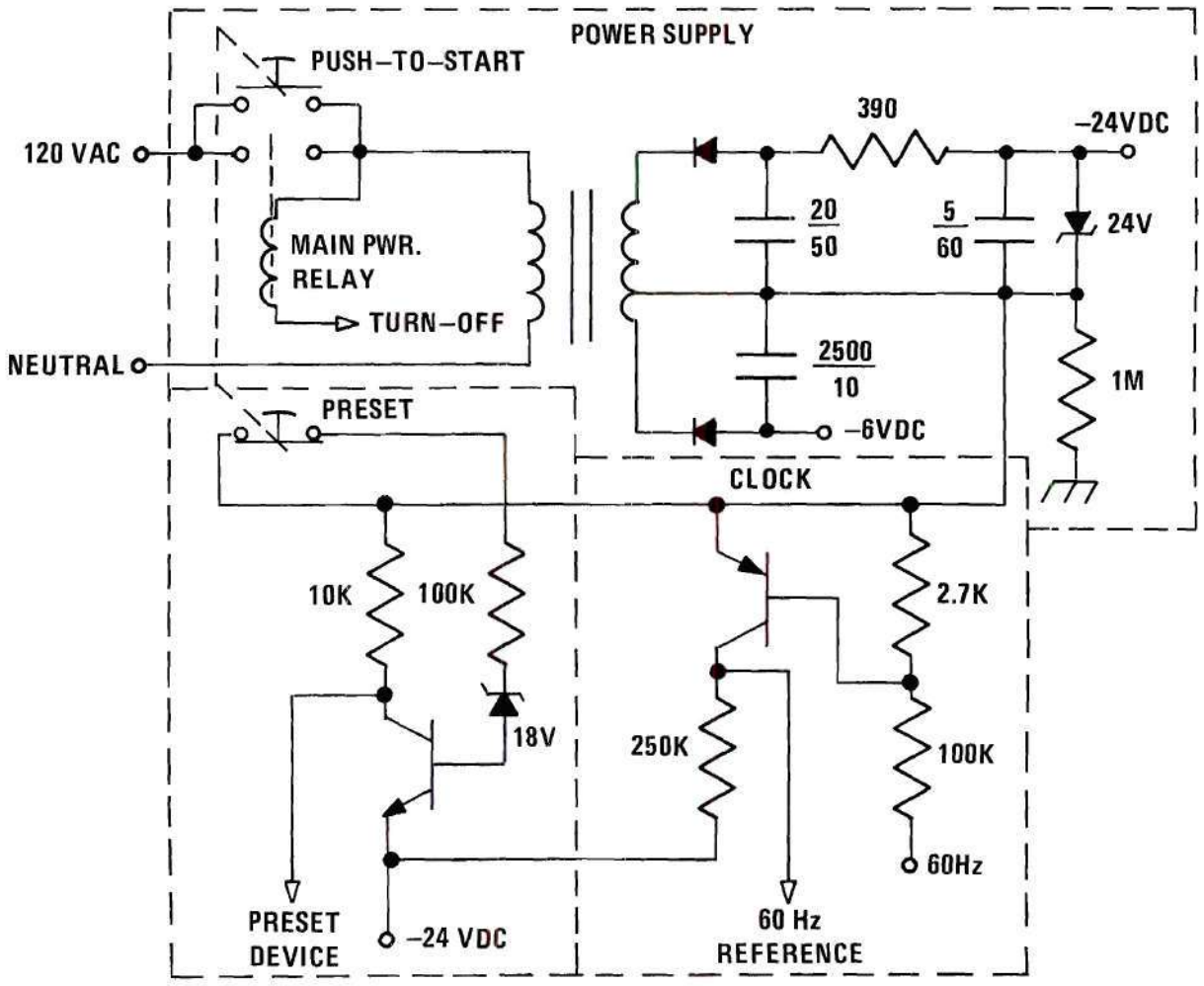
ELECTRONIC TIMER SCHEMATICS
Continued



Typical Indicator Lamp Output Driver Schematic

Description: The above circuit is used on the five indicator "lamps." When the MOS device output is on or grounded, the transistor is forward biased and current flows through the light emitting diode and the 270 ohm current limiting resistor.

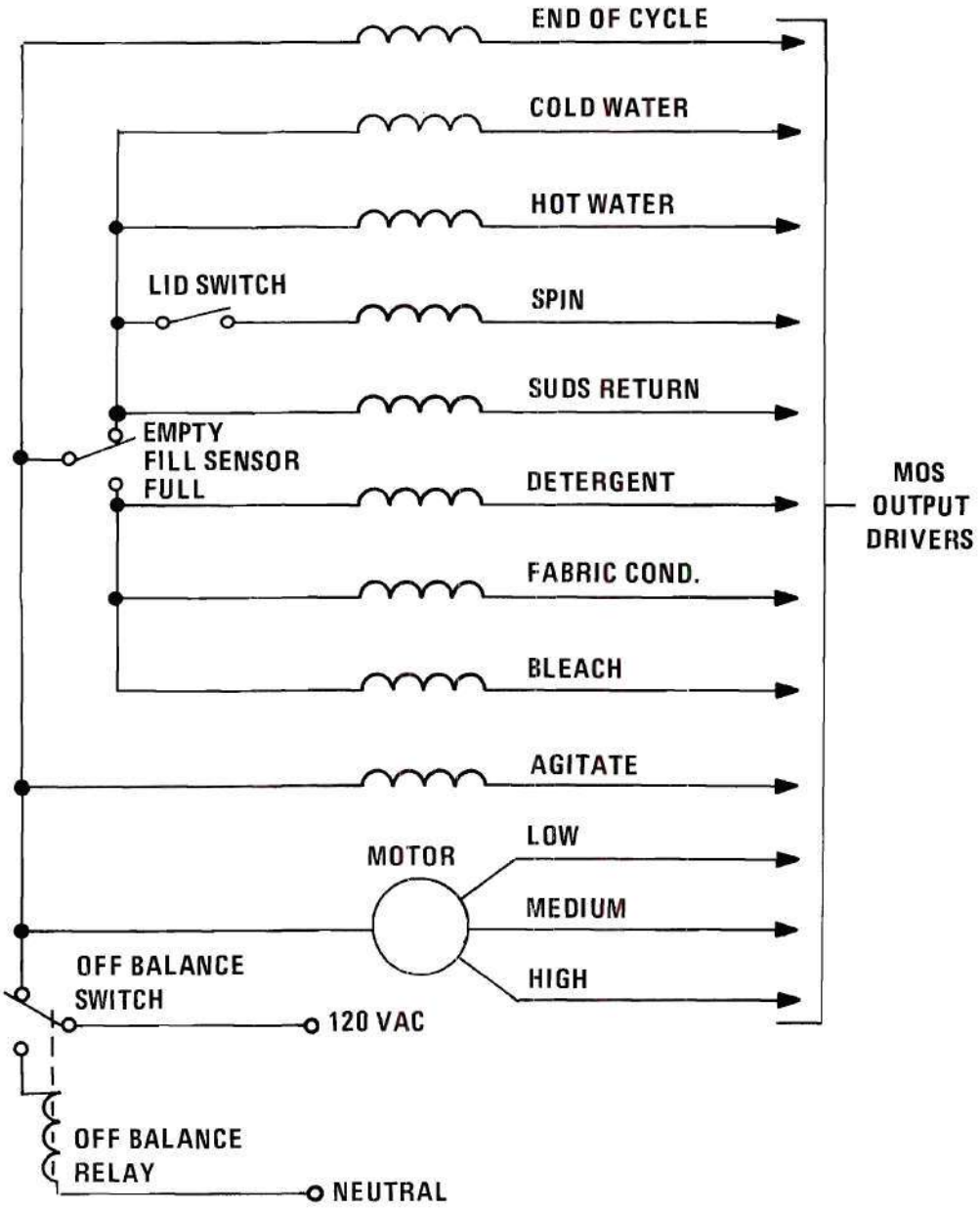
ELECTRONIC TIMER SCHEMATICS
Continued



Power Supply, Preset, and Clock Schematics

Description: The power supply is the standard center tapped, low voltage transformer with two rectifiers, filter capacitors, and a zener diode for regulation on the -24 volt side. The other side, -6 volts, supplies the output driver circuits. The push-to-start switch is a dual momentary switch which energizes the main power relay to supply 120 VAC to the transformer primary. The main power relay holds until the "Turn-Off Main Power" output of the MOS device comes on at the end of a cycle. The push-to-start switch also opens the base circuit of the preset transistor. This insures that the preset voltage comes up after the main power to the MOS device. The clock circuit provides a 60 hertz square wave for the MOS device reference.

ELECTRONIC TIMER SCHEMATICS
Continued

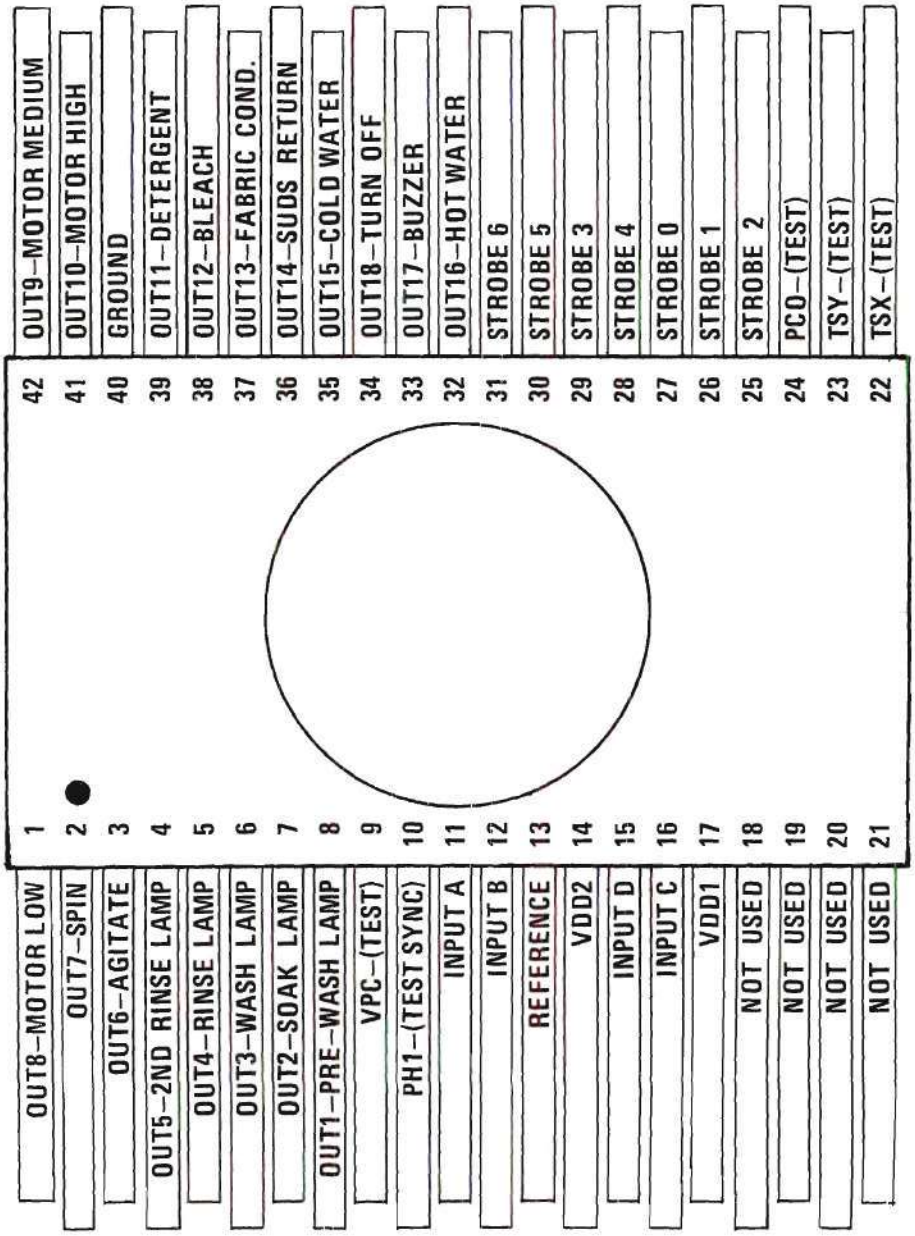


Control Elements Schematic

Description: The above circuit shows the control elements which are all 120 VAC elements. The lid switch breaks the spin solenoid line, the fill sensor not only indicates water level but prevents detergent, fabric conditioner, or bleach from going into an empty machine, and the off balance switch turns off all elements and holds until the machine is restarted.

APPENDIX B

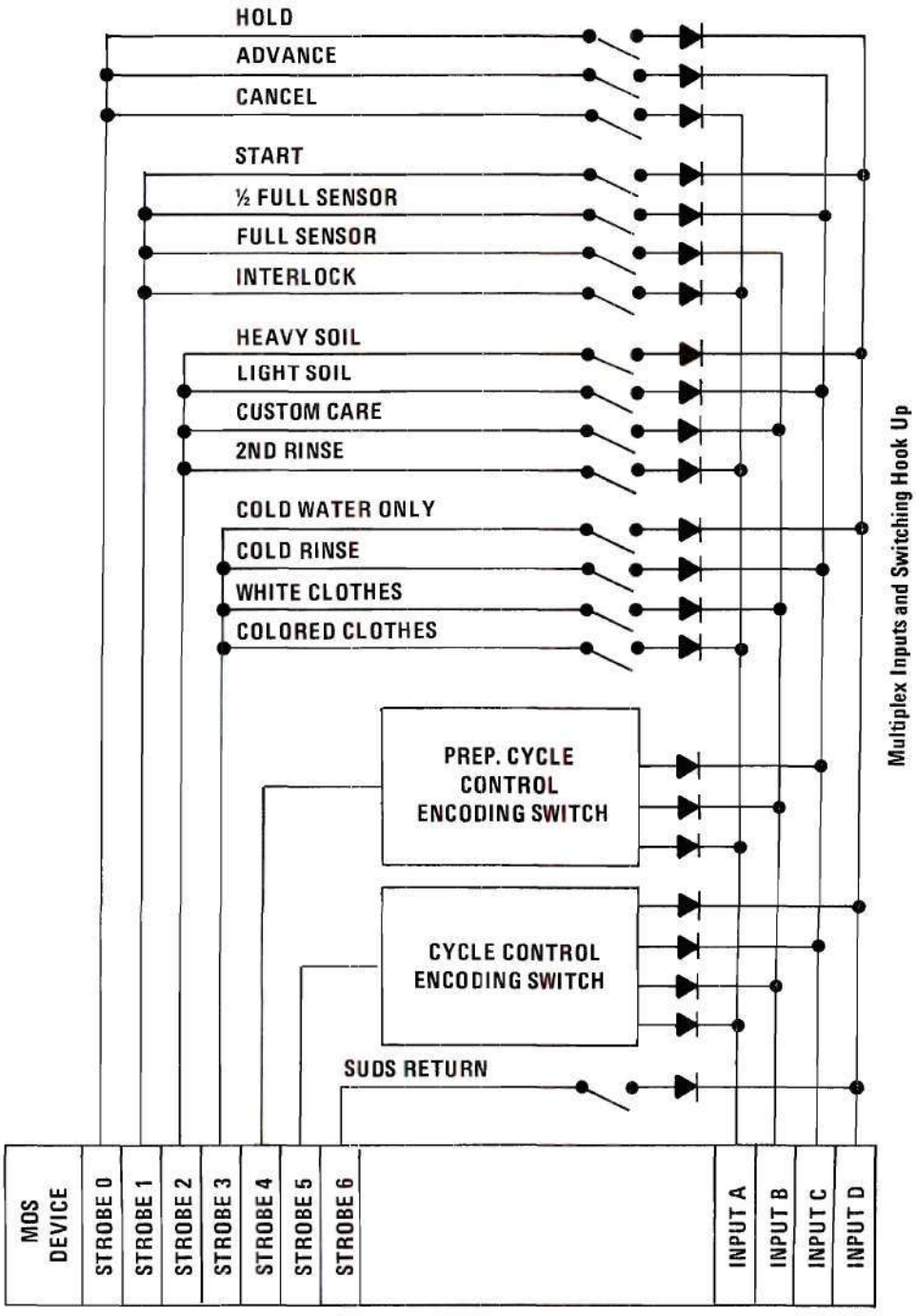
MOS DEVICE DETAILS



Pin Assignment

MOS DEVICE DETAILS

Continued



MOS DEVICE DETAILS
Continued

TABLE 1
Cycle Control Encoding
Strobe 5

Function	Input Line	A	B	C	D
Off		0	0	0	0
Heavy Fabric		X	X	0	0
Normal		X	0	X	0
Line Dry		0	X	X	0
Delicate		X	X	X	0
Very Delicate		0	0	X	0
Short Wash		0	X	0	X
Sanitize		X	0	0	X
Spin Only		0	0	0	X
Pump Only		X	X	0	X

Note: X - Input tied to corresponding strobe
0 - Input open

MOS DEVICE DETAILS
Continued

TABLE 2
Preparatory Cycle Control Encoding
Strobe 4

Function	Input Line	A	B	C	D
Off		0	0	0	
Pre-Wash		X	0	0	
Soak ½ Hour		0	X	0	
Soak 1 Hour		X	X	0	
Soak 2 Hours		0	X	X	
Soak 4 Hours		0	0	X	
Soak 8 hours		X	0	X	

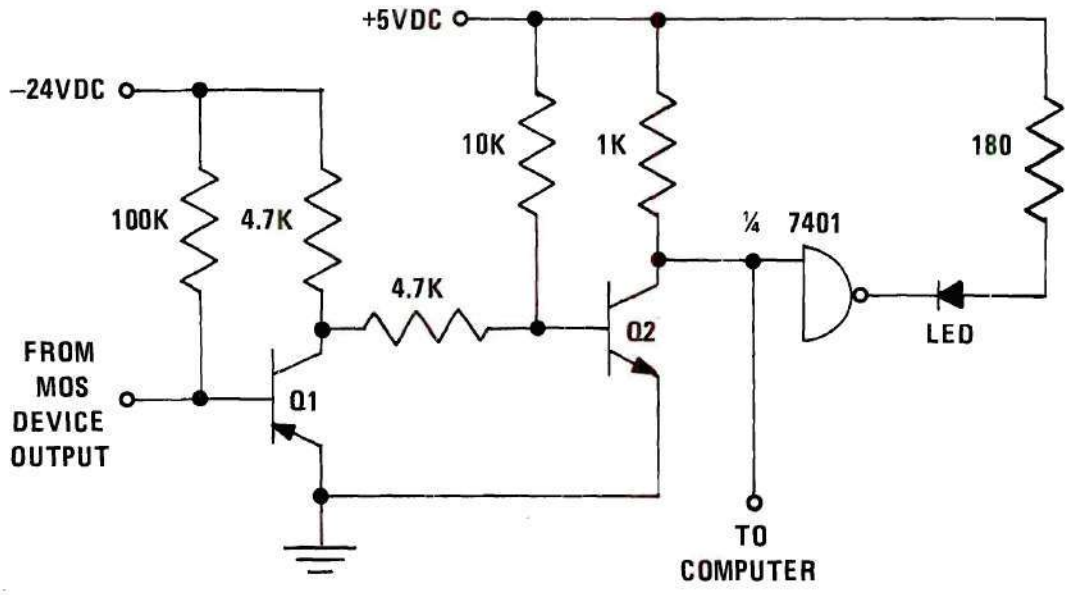
MOS DEVICE DETAILS
Continued

TABLE 3
Independent Control Encoding
Strobes 0, 1, 2, 3 and 6

	Function	Input Line	A	B	C	D
Strobe 6:	Suds Return		0	0	0	X
Strobe 3:	Colored Clothes		X	0	0	0
	White Clothes		0	X	0	0
	Cold Rinse		0	0	X	0
	Cold Water Only		0	0	0	X
Strobe 2:	2nd Rinse		X	0	0	0
	Custom Care		0	X	0	0
	Light Soil		0	0	X	0
	Heavy Soil		0	0	0	X
Strobe 1:	Interlock		X	0	0	0
	Full Sensor (FS)		0	X	0	0
	½ Full Sensor (HS)		0	0	X	0
	Start		0	0	0	X
Strobe 0:	Cancel		X	0	0	0
	Advance		0	0	X	0
	Hold		0	0	0	X

APPENDIX C

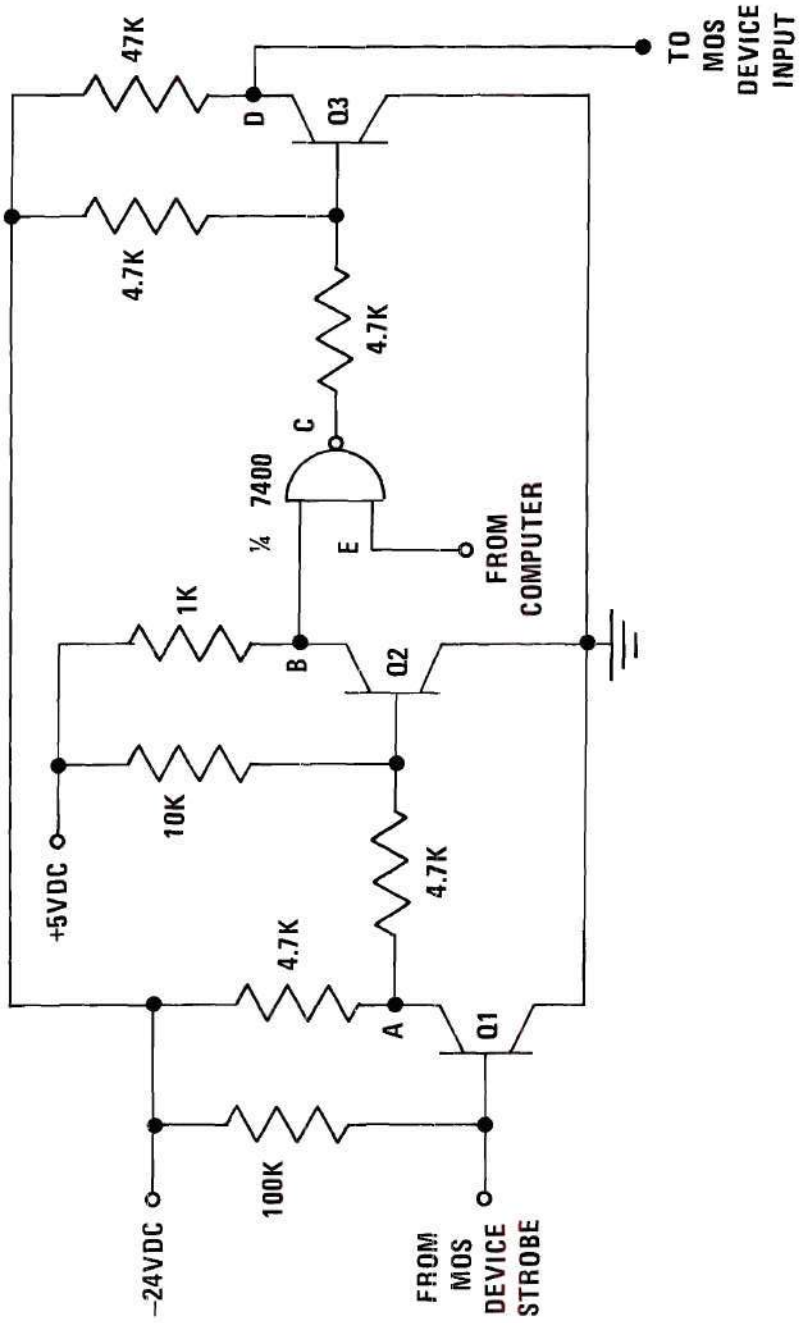
OUTPUT LEVEL TRANSLATOR SCHEMATIC



Description: The above circuit is used on the 18 MOS device outputs to translate the "on", 1000 ohms to ground, and "off", 10,000 ohms to gounrd, states of the MOS device to 0 and +5 volt levels for the computer. When the device output is off, Q1 is on through the 100K resistor, and the collector of Q1 is at ground. Q2 is on through the 10K resistor and its collector is also at ground or zero volts. The output to the computer is taken at the collector of Q2 and is therefore zero volts or off. This output is also connected to an open collector NAND gate which drives an LED. With one lead of the NAND gate open, current flows through the 180 ohm resistor and the LED only when the collector of Q2 is at +5 volts. When the device output is on, Q1 is not forward biased and its collector is at -24 volts. Now Q2 is reversed biased, its collector is at +5 volts, and the output to the computer is at +5 volts or on. Also, current flows through the LED to turn it on.

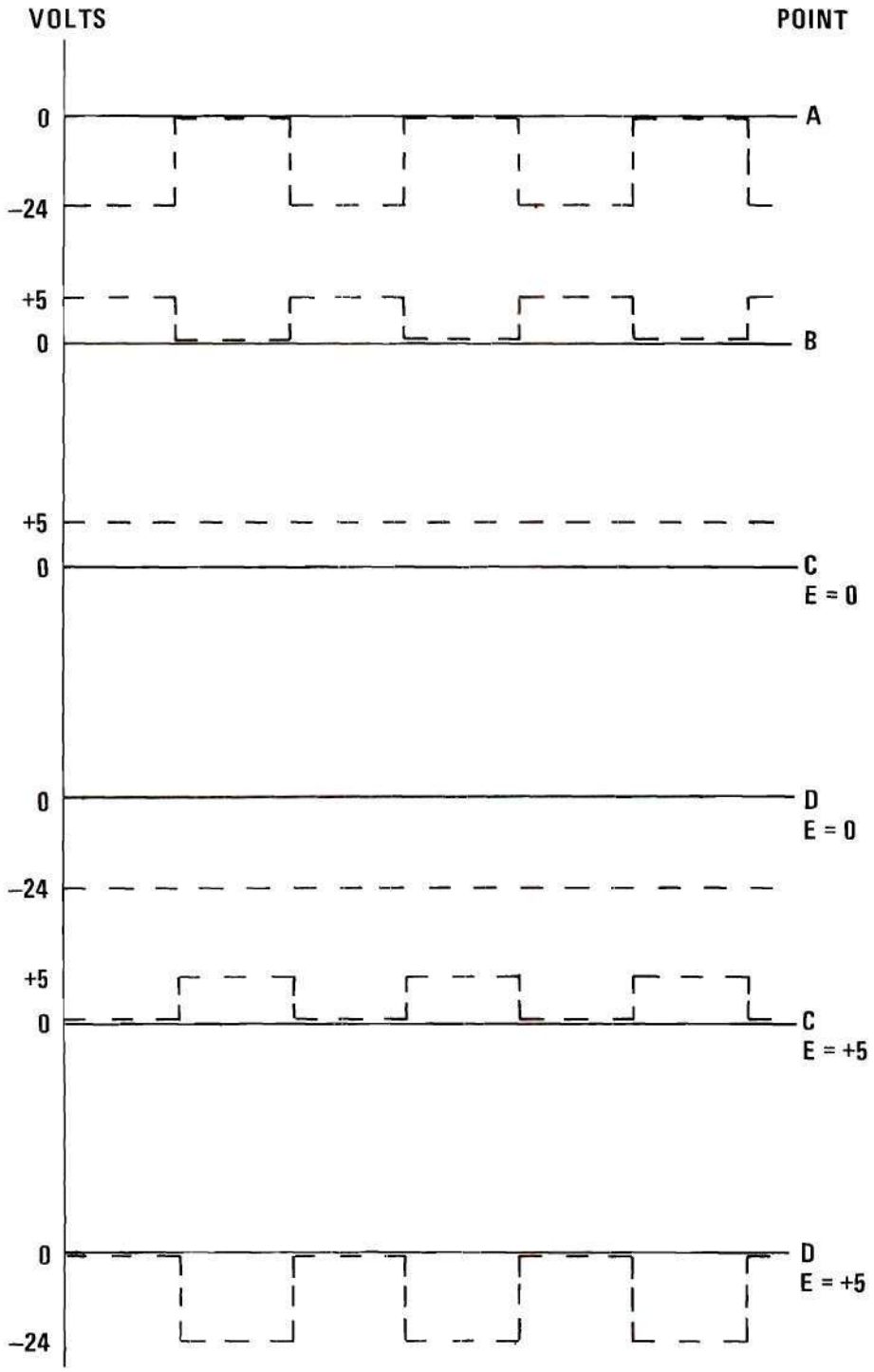
APPENDIX D

INPUT LEVEL TRANSLATOR SCHEMATIC



INPUT LEVEL TRANSLATOR SCHEMATIC

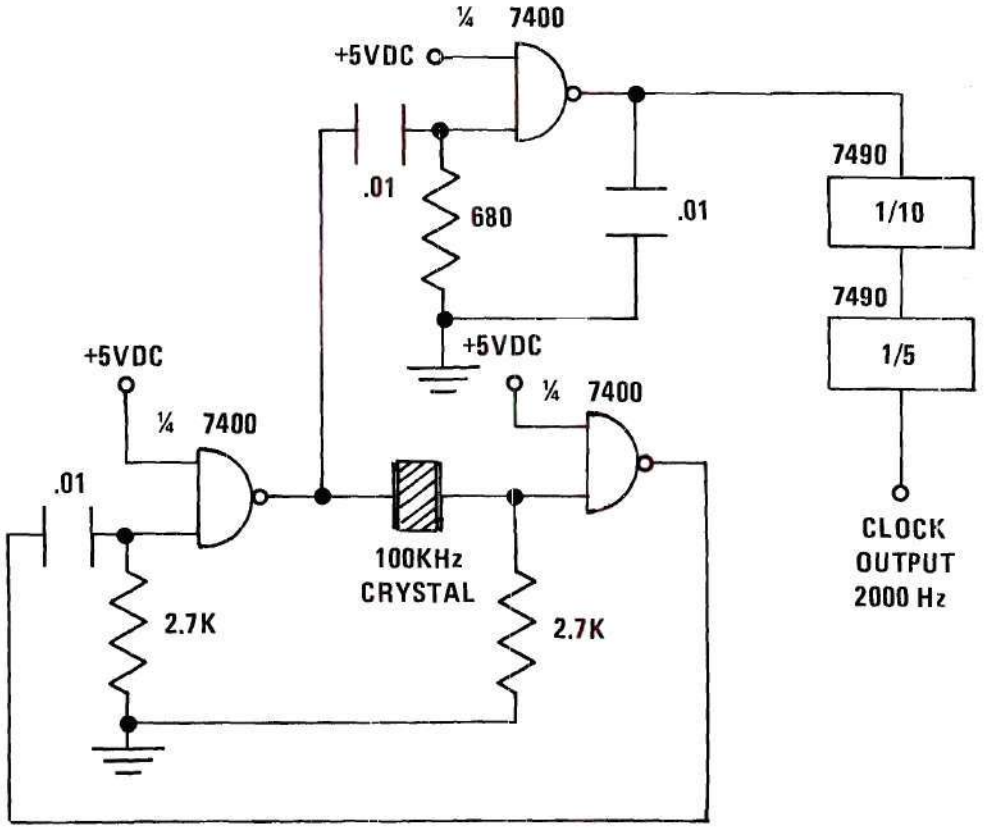
Continued



Description: The circuit is used on the 21 input lines (one each on Strobes 0 and 6, four each on Strobes 1, 2, 3, and 5, and three on Strobe 4) to allow the strobe signals to be coded by the computer into cycle selections. The plots show the waveforms at points A, B, C, D, and E on the schematic. When an input is to be on, point D sinks current from the device input just as the device strobe does. This action is controlled by a signal from the computer to the NAND gate on the schematic.

APPENDIX E

CRYSTAL CLOCK SCHEMATIC



APPENDIX F

COMPUTER PROGRAM

```
---
                ;PAGE ZERO
          000100 .LOC 100
   00100 000000 CN:     0        ;CYCLE NO.
   00101 000000 SN:     0        ;SEQUENCE NO.
   00102 000000 HPST:   0        ;HIGH PRESENT STATUS
   00103 000000 LPST:   0        ;LOW PRESENT STATUS
   00104 000000 HST:    0        ;HIGH STATUS
   00105 000000 LST:    0        ;LOW STATUS
   00106 000000 HDST:   0        ;HIGH DESIRED STATUS
   00107 000000 LDST:   0        ;LOW DESIRED STATUS
   00110 000002 OFF:    2        ;TURN OFF CHECK
   00111 003061 ICA:    IC       ;INPUT  CYCLE ADD.
   00112 003101 RSA:    RS       ;READ STATUS ADD.
   00113 003114 ISA:    IS       ;INCREMENT SEQUENCE NO. ADD.
   00114 003252 TOEA:   TOE      ;TIME OVERFLOW ERROR ADD.
   00115 003036 STCHA:  STCH     ;STATUS CHANGE
   00116 003271 STEA:   STE      ;STATUS ERROR ADD.
   00117 003313 TEA:    TE       ;TIME ERROR ADD.
   00120 003705 DSBA:   DSB      ;DESIRED STATUS BUF. ADD.
   00121 003016 LP1A:   LOOP1    ;LOOP1 ADD.
   00122 003035 LP2A:   LOOP2    ;LOOP2 ADD.
   00123 000000 RET1:   0        ;RETURN1
   00124 000000 RET2:   0        ;RETURN2
   00125 000400 DEBA:   400      ;DEBUG ADD.
   00126 003667 ICBA:   ICB      ;INPUT CYCLE BUFFER ADD.
   00127 000000 HCT:    0        ;HIGH COUNTER
   00130 000000 LCT:    0        ;LOW COUNTER
   00131 000006 HCTM:   6        ;HIGH COUNTER MAXIMUM
   00132 177777 LCTM:   177777   ;LOW COUNTER MAXIMUM
   00133 003037 NSCHA:  NSCH     ;NO STATUS CHANGE ADD.
   00134 000000 HUL:    0        ;HIGH UPPER COUNTER LIMIT
   00135 000000 LUL:    0        ;LOW UPPER COUNTER LIMIT
   00136 000000 HLL:    0        ;HIGH LOWER COUNTER LIMIT
   00137 000000 LLL:    0        ;LOW LOWER COUNTER LIMIT
   00140 004363 ULBA:   ULB      ;UPPER LIMIT BUFFER ADD.
   00141 005041 LLBA:   LLB      ;LOWER LIMIT BUFFER ADD.
   00142 003625 STPA:   STP      ;STATUS PRINT SUB. ADD.
   00143 003645 DSTPA:  DSTP     ;DESIRED STATUS PRINT SUB. ADD.
   00144 000000 RET3:   0        ;RETURN3
   00145 000000 RET4:   0        ;RETURN4
   00146 000040 PRST:   40       ;PRESET
   00147 003000 DLAY1:  3000     ;DELAY1
   00150 001000 DLAY2:  1000     ;DELAY2
   00151 003705 DSBA1:  DSB      ;DESIRED STATUS BUF. START ADD.
   00152 003667 ICBA1:  ICB      ;INPUT CYCLE BUF. START ADD.
   00153 004363 ULBA1:  ULB      ;UPPER LIMITS BUF. START ADD.
   00154 005041 LLBA1:  LLB      ;LOWER LIMITS BUF. START ADD.
                ;MAIN PROGRAM
          003000 .LOC 3000
   03000 102400 START:  SUB      0,0      ;AC0=0
   03001 040100         STA      0,CN     ;CYCLE NO.=0
   03002 061040         DOA      0,40     ;ZERO HIGH INPUT
   03003 062040         DOB      0,40     ;ZERO LOW INPUT
   03004 020147         LDA      0,DLAY1  ;AC0=DELAY1
   03005 006057         JSR      @,SDE2   ;DELAY 3 SECONDS
   03006 020151         LDA      0,DSBA1  ;AC0=DES. STATUS BUF. START
   03007 040120         STA      0,DSBA   ;DES. STATUS BUF.=START ADD.
  03010 020152          LDA      0,ICBA1  ;AC0=INPUT CYC. BUF. START
   03011 040126         STA      0,ICBA   ;INPUT CYC. BUF.=START ADD.
   03012 020153         LDA      0,ULBA1  ;AC0=UPPER LIM. BUF. START
```

```
---
03013 040140          STA     0,ULBA  ;UPPER LIM. BUF.=START ADD.
03014 020154          LDA     0,LLBA1 ;AC0=LOWER LIM. BUF. START
03015 040141          STA     0,LLBA  ;LOWER LIM. BUF.=START ADD.
03016 102400 LOOP1:   SUB     0,0     ;AC0=0
03017 040101          STA     0,SN    ;SEQUENCE NO.=0
03020 040127          STA     0,HCT   ;HIGH COUNTER=0
03021 040130          STA     0,LCT   ;LOW COUNTER=0
03022 040102          STA     0,HPST  ;HIGH PRESENT STATUS=0
03023 040103          STA     0,LPST  ;LOW PRESENT STATUS=0
03024 040104          STA     0,HST   ;HIGH STATUS=0
03025 040105          STA     0,LST   ;LOW STATUS=0
03026 040106          STA     0,HDST  ;HIGH DESIRED STATUS=0
03027 040107          STA     0,LDST  ;LOW DESIRED STATUS=0
03030 040134          STA     0,HUL   ;HIGH UPPER COUNTER LIMIT=0
03031 040135          STA     0,LUL   ;LOW UPPER COUNTER LIMIT=0
03032 040136          STA     0,HLL   ;HIGH LOWER COUNTER LIMIT=0
03033 040137          STA     0,LLL   ;LOW LOWER COUNTER LIMIT=0
03034 006111          JSR     @,ICA   ;INPUT CYCLE SUB.
03035 006112 LOOP2:   JSR     @,RSA   ;READ STATUS SUB.
03036 006113 STCH:    JSR     @,ISA   ;INCREMENT SEQUENCE SUB.
03037 020130 NSCH:    LDA     0,LCT   ;AC0=LOW COUNTER
03040 024132          LDA     1,LCTM  ;AC1=LOW COUNTER MAXIMUM
03041 106414          SUB#    0,1,SZR ;IS LO CTR.=LO CTR. MAX.
03042 000415          JMP     ILCT    ;NO, JUMP TO INC. LO CTR.
03043 102400          SUB     0,0     ;YES, AC0=0
03044 040130          STA     0,LCT   ;LOW COUNTER=0
03045 010127          ISZ     HCT     ;INCREMENT HIGH COUNTER
03046 020130 RET:     LDA     0,LCT   ;AC0=LOW COUNTER
03047 024132          LDA     1,LCTM  ;AC1=LOW COUNTER MAXIMUM
03050 106414          SUB#    0,1,SZR ;IS LO CTR.=LO CTR. MAX.
03051 000764          JMP     LOOP2   ;NO, RETURN
03052 020127          LDA     0,HCT   ;YES, AC0=HIGH COUNTER
03053 024131          LDA     1,HCTM  ;AC1=HIGH COUNTER MAXIMUM
03054 106414          SUB#    0,1,SZR ;IS HI CTR.=HI CTR. MAX.
03055 000760          JMP     LOOP2   ;NO, RETURN
03056 006114          JSR     @,TOEA  ;YES, TIME OVERFLOW ERROR
03057 010130 ILCT:    ISZ     LCT     ;INCREMENT LOW COUNTER
03060 000766          JMP     RET     ;RETURN
                ;INPUT CYCLE SUBROUTINE
03061 054123 IC:      STA     3,RET1  ;RETURN1=AC3
03062 030126          LDA     2,ICBA  ;AC2=INPUT CYCLE BUFFER
03063 020146          LDA     0,PRST  ;AC0=PRESET
03064 062040          DOB     0,40    ;SEND PRESET TO DEVICE
03065 020150          LDA     0,DLAY2 ;AC0=DELAY2
03066 006057          JSR     @,SDE2  ;DELAY 1 SECOND
03067 020100          LDA     0,CN    ;AC0=CYCLE NO.
03070 101120          MOVZL   0,0     ;MULTIPLY CN BY 2
03071 113000          ADD     0,2     ;AC0+AC2
03072 021000          LDA     0,0,2   ;AC0=HIGH INPUT
03073 025001          LDA     1,1,2   ;AC1=LOW INPUT
03074 101005          MOV     0,0,SNR ;IS AC0=0
03075 002125          JMP     @,DEBA  ;YES, JUMP TO DEBUG
03076 061040          DOA     0,40    ;NO, SEND HIGH INPUT TO DEVICE
03077 066040          DOB     1,40    ;SEND LOW INPUT TO DEVICE
03100 002123          JMP     @,RET1  ;RETURN
```

```
---
                ;READ STATUS SUBROUTINE
  03101 060440 RS:      DIA     0,40    ;GET HIGH STATUS FROM DEVICE
  03102 065440          DIB     1,40    ;GET LOW STATUS FROM DEVICE
  03103 040104          STA     0,HST   ;HIGH STATUS=AC0
  03104 044105          STA     1,LST   ;LOW STATUS=AC1
  03105 030102          LDA     2,HPST  ;AC2=HIGH PRESENT STATUS
  03106 034103          LDA     3,LPST  ;AC3=LOW PRESENT STATUS
  03107 112414          SUB#    0,2,SZR ;IS HI STATUS=HI PRES. STATUS
  03110 002115          JMP     @,STCHA ;NO, STATUS CHANGE
  03111 136414          SUB#    1,3,SZR ;YES, IS LO STAT.=LO PRES. STAT.
  03112 002115          JMP     @,STCHA ;NO, STATUS CHANGE
  03113 002133          JMP     @,NSCHA ;YES, RETURN
                ;INCREMENT SEQUENCE SUBROUTINE
  03114 054124 IS:      STA     3,RET2  ;RETURN2=AC3
  03115 030120          LDA     2,DSBA  ;AC2=DESIRED STATUS BUFFER
  03116 020101          LDA     0,SN    ;AC0=SEQUENCE NO.
  03117 101120          MOVZL   0,0     ;MULTIPLY SN BY 2
  03120 113000          ADD     0,2     ;AC0+AC2
  03121 021000          LDA     0,0,2   ;AC0=HIGH DESIRED STATUS
  03122 025001          LDA     1,1,2   ;AC1=LOW DESIRED STATUS
  03123 040106          STA     0,HDST  ;HIGH DESIRED STATUS=AC0
  03124 044107          STA     1,LDST  ;LOW DESIRED STATUS=AC1
  03125 030104          LDA     2,HST   ;AC2=HIGH STATUS
  03126 034105          LDA     3,LST   ;AC3=LOW STATUS
  03127 112414          SUB#    0,2,SZR ;IS HI STATUS=HI DES. STATUS
  03130 006116          JSR     @,STEA  ;NO, STATUS ERROR
  03131 136414          SUB#    1,3,SZR ;YES,IS LO STAT.=LO DES. STAT.
 03132 006116          JSR     @,STEA  ;NO, STATUS ERROR
  03133 030140          LDA     2,ULBA  ;YES, AC2=UPPER LIM. BUF. ADD.
 03134 020101          LDA     0,SN    ;AC0=SEQUENCE NO.
  03135 101120          MOVZL   0,0     ;MULTIPLY SN BY 2
  03136 113000          ADD     0,2     ;AC0+AC2
  03137 021000          LDA     0,0,2   ;AC0=HIGH UPPER COUNTER LIMIT
  03140 025001          LDA     1,1,2   ;AC1=LOW UPPER COUNTER LIMIT
  03141 040134          STA     0,HUL   ;HIGH UPPER COUNTER LIMIT=AC0
  03142 044135          STA     1,LUL   ;LOW UPPER COUNTER LIMIT=AC1
  03143 030141          LDA     2,LLBA  ;AC2=LOWER LIMITS BUFFER ADD.
  03144 020101          LDA     0,SN    ;AC0=SEQUENCE NO.
  03145 101120          MOVZL   0,0     ;MULTIPLY SN BY 2
  03146 113000          ADD     0,2     ;AC0+AC2
  03147 021000          LDA     0,0,2   ;AC0=HIGH LOWER COUNTER LIMIT
  03150 025001          LDA     1,1,2   ;AC1=LOW LOWER COUNTER LIMIT
  03151 040136          STA     0,HLL   ;HIGH LOWER COUNTER LIMIT=AC0
  03152 044137          STA     1,LLL   ;LOW LOWER COUNTER LIMIT=AC1
  03153 020127          LDA     0,HCT   ;AC0=HIGH COUNTER
  03154 024134          LDA     1,HUL   ;AC1=HIGH UPPER COUNTER LIMIT
  03155 122432          SUBZ#   1,0,SZC ;IS HI UPPER CTR. LIM.>HI CTR.
  03156 000402          JMP     CHEQ1   ;NO, CHECK EQUALITY 1
  03157 000407          JMP     CHLL    ;YES, CHECK LOWER COUNTER LIMIT
  03160 122414 CHEQ1:   SUB#    1,0,SZR ;IS HI UPPER CTR. LIM.=HI CTR.
  03161 006117          JSR     @,TEA   ;NO, TIME ERROR
  03162 020130          LDA     0,LCT   ;YES, AC0=LOW COUNTER
  03163 024135          LDA     1,LUL   ;AC1=LOW UPPER COUNTER LIMIT
  03164 122032          ADCZ#   1,0,SZC ;IS LO UPPER CTR. LIM.>=LO CTR.
  03165 006117          JSR     @,TEA   ;NO, TIME ERROR
  03166 020127 CHLL:    LDA     0,HCT   ;YES, AC0=HIGH COUNTER
  03167 024136          LDA     1,HLL   ;AC1=HIGH LOWER COUNTER LIMIT
  03170 106432          SUBZ#   0,1,SZC ;IS HI CTR.>HI LOWER CTR. LIM.
  03171 000452          JMP     CHEQ2   ;NO, CHECK EQUALITY 2
  03172 020105 CTOK:    LDA     0,LST   ;YES, AC0=LOW STATUS
```

```
---
  03173 024110          LDA     1,OFF    ;AC1=OFF
  03174 107404          AND     0,1,SZR  ;IS TURN-OFF OFF
  03175 000412          JMP     ICN      ;NO, JUMP TO INCREMENT CYCLE NO.
  03176 010101          ISZ     SN       ;YES, INCREMENT SEQUENCE NO.
 03177 020106          LDA     0,HDST   ;AC0=HIGH DESIRED STATUS
  03200 024107          LDA     1,LDST   ;AC1=LOW DESIRED STATUS
  03201 040102          STA     0,HPST   ;HIGH PRESENT STATUS=AC0
  03202 044103          STA     1,LPST   ;LOW PRESENT STATUS=AC1
  03203 102400          SUB     0,0      ;AC0=0
  03204 040127          STA     0,HCT    ;HIGH COUNTER=0
  03205 040130          STA     0,LCT    ;LOW COUNTER=0
  03206 002122          JMP     @,LP2A   ;RETURN TO LOOP2
  03207 102400 ICN:     SUB     0,0      ;AC0=0
  03210 061040          DOA     0,40     ;ZERO HIGH INPUT
  03211 062040          DOB     0,40     ;ZERO LOW INPUT
  03212 020147          LDA     0,DLAY1  ;AC0=DELAY1
  03213 006057          JSR     @,SDE2   ;DELAY 3 SECONDS
  03214 010100          ISZ     CN       ;INCREMENT CYCLE NO.
  03215 020120          LDA     0,DSBA   ;AC0=DESIRED STATUS BUFFER ADD.
  03216 024101          LDA     1,SN     ;AC1=SEQUENCE NO.
  03217 125120          MOVZL   1,1
  03220 107000          ADD     0,1      ;AC0+AC1
  03221 125400          INC     1,1      ;INCREMENT AC1
  03222 125400          INC     1,1      ;INCREMENT AC1
  03223 044120          STA     1,DSBA   ;DESIRED STATUS BUFFER ADD.=AC1
  03224 020140          LDA     0,ULBA   ;AC0=UPPER LIMIT BUFFER ADD.
  03225 024101          LDA     1,SN     ;AC1=SEQUENCE NO.
  03226 125120          MOVZL   1,1
  03227 107000          ADD     0,1      ;AC0+AC1
  03230 125400          INC     1,1      ;INCREMENT AC1
  03231 125400          INC     1,1      ;INCREMENT AC1
  03232 044140          STA     1,ULBA   ;UPPER LIMIT BUFFER ADD.=AC1
  03233 020141          LDA     0,LLBA   ;AC0=LOWER LIMIT BUFFER ADD.
  03234 024101          LDA     1,SN     ;AC1=SEQUENCE NO.
  03235 125120          MOVZL   1,1
  03236 107000          ADD     0,1      ;AC0+AC1
  03237 125400          INC     1,1      ;INCREMENT AC1
  03240 125400          INC     1,1      ;INCREMENT AC1
  03241 044141          STA     1,LLBA   ;LOWER LIMIT BUFFER ADD.=AC1
  03242 002121          JMP     @,LP1A   ;RETURN TO LOOP1
  03243 122414 CHEQ2:   SUB#    1,0,SZR  ;IS HI CTR.=HI LOWER CTR. LIM.
  03244 006117          JSR     @,TEA    ;NO, TIME ERROR
  03245 020130          LDA     0,LCT    ;YES, AC0=LOW COUNTER
  03246 024137          LDA     1,LLL    ;AC1=LOW LOWER COUNTER LIMIT
 03247 106032          ADCZ#   0,1,SZC  ;IS LO CTR.>=LO LOWER CTR. LIM.
  03250 006117          JSR     @,TEA    ;NO, TIME ERROR
  03251 000721          JMP     CTOK     ;YES,RETURN TO COUNTER OK
```

```
---
                    ;ERROR SUBROUTINES
   03252 006043 TOE:    JSR     0,SBT    ;BLOCK TRANSFER SUB.
   03253 003365         MES1             ;MESSAGE 1
   03254 006043         JSR     0,SBT
   03255 003402         MES2
   03256 024100         LDA     1,CN     ;AC1=CYCLE NO.
   03257 006053         JSR     0,BIND   ;BINARY TO DECIMAL SUB.
   03260 006043         JSR     0,SBT
   03261 003417         MES3
   03262 024101         LDA     1,SN     ;AC1=SEQUENCE NO.
   03263 006053         JSR     0,BIND
   03264 006043         JSR     0,SBT
   03265 003434         MES4
   03266 006142         JSR     0,STPA   ;STATUS PRINT SUB.
   03267 006062         JSR     0,SPCL   ;PRINT,CR, LF SUB.
   03270 002125         JMP     0,DEBA   ;DEBUG SUB.
   03271 006043 STE:    JSR     0,SBT
   03272 003451         MES5
   03273 006043         JSR     0,SBT
   03274 003402         MES2
   03275 024100         LDA     1,CN     ;AC1=CYCLE NO.
   03276 006053         JSR     0,BIND
   03277 006043         JSR     0,SBT
   03300 003417         MES3
   03301 024101         LDA     1,SN     ;AC1=SEQUENCE NO.
   03302 006053         JSR     0,BIND
   03303 006043         JSR     0,SBT
   03304 003434         MES4
   03305 006142         JSR     0,STPA   ;STATUS PRINT SUB.
U  03306 006400         JSR     0,S0T
   03307 003462         MES6
   03310 006143         JSR     0,DSTPA  ;DESIRED STATUS PRINT SUB.
   03311 006062         JSR     0,SPCL
   03312 002125         JMP     0,DEBA
   03313 006043 TE:     JSR     0,SBT
   03314 003477         MES7
   03315 006043         JSR     0,SBT
   03316 003402         MES2
   03317 024100         LDA     1,CN     ;AC1=CYCLE NO.
   03320 006053         JSR     0,BIND
   03321 006043         JSR     0,SBT
   03322 003417         MES3
   03323 024101         LDA     1,SN     ;AC1=SEQUENCE NO.
   03324 006053         JSR     0,BIND
   03325 006043         JSR     0,SBT
   03326 003434         MES4
   03327 006142         JSR     0,STPA   ;STATUS PRINT SUB.
   03330 006043         JSR     0,SBT
   03331 003462         MES6
   03332 006143         JSR     0,DSTPA  ;DESIRED STATUS PRINT SUB.
   03333 006043         JSR     0,SBT
   03334 003507         MES8
   03335 024134         LDA     1,HUL    ;AC1=HIGH UPPER COUNTER LIMIT
   03336 006052         JSR     0,BINO   ;BINARY TO OCTAL SUB.
   03337 006043         JSR     0,SBT
   03340 003524         MES9
   03341 024135         LDA     1,LUL    ;AC1=LOW UPPER COUNTER LIMIT
   03342 006052         JSR     0,BINO
   03343 006043         JSR     0,SBT
   03344 003541         MES10
```

```
---
   03345 024127          LDA     1,HCT   ;AC1=HIGH COUNTER
   03346 006052          JSR     @,BINO
   03347 006043          JSR     @,SBT
   03350 003556          MES11
   03351 024130          LDA     1,LCT   ;AC1=LOW COUNTER
   03352 006052          JSR     @,BINO
   03353 006043          JSR     @,SBT
   03354 003573          MES12
   03355 024136          LDA     1,HLL   ;AC1=HIGH LOWER COUNTER LIMIT
  03356 006052          JSR     @,BINO
   03357 006043          JSR     @,SBT
   03360 003610          MES13
   03361 024137          LDA     1,LLL   ;AC1=LOW LOWER COUNTER LIMIT
   03362 006052          JSR     @,BINO
   03363 006062          JSR     @,SPCL
   03364 006125          JSR     @,DEBA
         000043 SBT=43
         000053 BIND=53
         000062 SPCL=62
         000044 SBNP=44
         000057 SDE2=57
         000052 BINO=52
   03365 005015 MES1:    .TXT/<15><12>
   03366 020040
   03367 052052 *T
   03370 046511 IM
   03371 020105 E
   03372 053117 OV
   03373 051105 ER
   03374 046106 FL
   03375 053517 OW
   03376 042440  E
   03377 051122 RR
   03400 051117 OR
   03401 000000 /

   03402 005015 MES2:    .TXT/<15><12>
   03403 020040
   03404 054503 CY
   03405 046103 CL
   03406 020105 E
   03407 047516 NO
   03410 036456 .=
   03411 027056 ..
   03412 027056 ..
   03413 027056 ..
   03414 027056 ..
   03415 027056 ..
   03416 000000 /

   03417 005015 MES3:    .TXT/<15><12>
   03420 020040
   03421 042523 SE
   03422 052521 QU
   03423 047105 EN
   03424 042503 CE
   03425 047040  N
   03426 027117 O.
   03427 027075 =.
   03430 027056 ..
```

```
---
   03431 027056 ..
   03432 027056 ..
   03433 000000 /

   03434 005015 MES4:   .TXT/<15><12>
   03435 020040
   03436 052123 ST
   03437 052101 AT
   03440 051525 US
   03441 027075 =.
   03442 027056 ..
   03443 027056 ..
   03444 027056 ..
   03445 027056 ..
   03446 027056 ..
   03447 027056 ..
   03450 000056 ./

   03451 005015 MES5:   .TXT/<15><12>
   03452 020040
   03453 051452 *S
   03454 040524 TA
   03455 052524 TU
   03456 020123 S
   03457 051105 ER
   03460 047522 RO
   03461 000122 R/

   03462 005015 MES6:   .TXT/<15><12>
   03463 020040
   03464 042504 DE
   03465 044523 SI
   03466 042522 RE
   03467 020104 D
   03470 052123 ST
   03471 052101 AT
   03472 051525 US
   03473 027075 =.
   03474 027056 ..
   03475 027056 ..
   03476 000056 ./

   03477 005015 MES7:   .TXT/<15><12>
   03500 020040
   03501 052052 *T
   03502 046511 IM
   03503 020105 E
   03504 051105 ER
   03505 047522 RO
   03506 000122 R/

   03507 005015 MES8:   .TXT/<15><12>
   03510 020040
   03511 044510 HI
   03512 044107 GH
   03513 052440  U
   03514 050120 PP
   03515 051105 ER
   03516 046040  L
   03517 046511 IM
```

```
---
   03520 052111 IT
   03521 027075 =.
   03522 027056 ..
   03523 000056 ./

   03524 005015 MES9:    .TXT/<15><12>
   03525 020040
   03526 047514 LO
   03527 020127 W
   03530 050125 UP
   03531 042520 PE
   03532 020122 R
   03533 044514 LI
   03534 044515 MI
   03535 036524 T=
   03536 027056 ..
   03537 027056 ..
   03540 000056 ./

   03541 005015 MES10:   .TXT/<15><12>
   03542 020040
   03543 044510 HI
   03544 044107 GH
   03545 041440  C
   03546 052517 OU
   03547 052116 NT
   03550 051105 ER
   03551 027075 =.
   03552 027056 ..
   03553 027056 ..
   03554 027056 ..
   03555 000056 ./

   03556 005015 MES11:   .TXT/<15><12>
   03557 020040
   03560 047514 LO
   03561 020127 W
   03562 047503 CO
   03563 047125 UN
   03564 042524 TE
   03565 036522 R=
   03566 027056 ..
   03567 027056 ..
   03570 027056 ..
   03571 027056 ..
   03572 000056 ./

   03573 005015 MES12:   .TXT/<15><12>
   03574 020040
   03575 044510 HI
   03576 044107 GH
   03577 046040  L
   03600 053517 OW
   03601 051105 ER
   03602 046040  L
   03603 046511 IM
   03604 052111 IT
   03605 027075 =.
   03606 027056 ..
   03607 000056 ./
```

```
---

 03610 005015 MES13:  .TXT/<15><12>
 03611 020040
 03612 047514 LO
 03613 020127 W
 03614 047514 LO
 03615 042527 WE
 03616 020122 R
 03617 044514 LI
 03620 044515 MI
 03621 036524 T=
 03622 027056 ..
 03623 027056 ..
 03624 000056 ./

              ;STATUS PRINT AND DESIRED STATUS PRINT SUBROUTINES
 03625 054144 STP:    STA     3,RET3  ;RETURN3=AC3
 03626 024105         LDA     1,LST   ;AC1=LOW STATUS
 03627 020437         LDA     0,ASC0  ;AC0=ASC0
 03630 030435         LDA     2,C2    ;AC2=C2
 03631 147414         AND#    2,1,SZR ;IS AC2=AC1
 03632 101400         INC     0,0     ;NO, INCREMENT AC0
 03633 006041         JSR     @,STT0  ;YES, JUMP TO TELETYPE OUT SUB.
03634 151220         MOVZR   2,2
 03635 024105         LDA     1,LST   ;AC1=LOW STATUS
 03636 020430         LDA     0,ASC0  ;AC0=ASC0
 03637 147414         AND#    2,1,SZR ;IS AC2=AC1
 03640 101400         INC     0,0     ;NO, INCREMENT AC0
 03641 006041         JSR     @,STT0  ;YES, JUMP TO TELETYPE OUT SUB.
03642 024104         LDA     1,HST   ;AC1=HIGH STATUS
 03643 006044         JSR     @,SBNP  ;BINARY PRINT SUB.
 03644 002144         JMP     @,RET3  ;RETURN
 03645 054145 DSTP:   STA     3,RET4  ;RETURN4=AC3
 03646 024107         LDA     1,LDST  ;AC1=LOW DESIRED STATUS
 03647 020417         LDA     0,ASC0  ;AC0=ASC0
 03650 030415         LDA     2,C2    ;AC2=C2
 03651 147414         AND#    2,1,SZR ;IS AC2=AC1
 03652 101400         INC     0,0     ;NO, INCREMENT AC0
 03653 006041         JSR     @,STT0  ;YES, JUMP TO TELETYPE OUT SUB.
03654 151220         MOVZR   2,2
 03655 024107         LDA     1,LDST  ;AC1=LOW DESIRED STATUS
 03656 020410         LDA     0,ASC0  ;AC0=ASC0
 03657 147414         AND#    2,1,SZR ;IS AC2=AC1
 03660 101400         INC     0,0     ;NO, INCREMENT AC0
 03661 006041         JSR     @,STT0  ;YES, JUMP TO TELETYPE OUT SUB.
03662 024106         LDA     1,HDST  ;AC1=HIGH DESIRED STATUS
 03663 006044         JSR     @,SBNP  ;BINARY PRINT SUB.
 03664 002145         JMP     @,RET4  ;RETURN
 03665 000002 C2:     2
 03666 000060 ASC0:   60
       000041 STT0=41
```

```
---
                ;INPUT CYCLE BUFFER
03667 000024 ICB:     24        ;START, FULL
03670 000043          43        ;PRESET, HEAVY FABRIC
03671 030024          30024     ;START, FULL, PREWASH, COLD WATER ONLY
03672 000042          42        ;PRESET, SHORT WASH
03673 000024          24        ;START, FULL
03674 000051          51        ;PRESET, SANITIZE
      000010 .BLK 10
                ;DESIRED STATUS BUFFER
03705 000004 DSB:     4
03706 000000          0
03707 140004          140004
03710 000000          0
03711 000004          4
03712 000000          0
03713 001044          1044
03714 000000          0
03715 003044          3044
03716 000000          0
03717 001044          1044
03720 000000          0
03721 005044          5044
03722 000000          0
03723 004004          4004
03724 000000          0
03725 004204          4204
03726 000000          0
03727 004004          4004
03730 000000          0
03731 000004          4
03732 000000          0
03733 020004          20004
03734 000000          0
03735 021004          21004
03736 000000          0
03737 020004          20004
03740 000000          0
03741 020204          20204
03742 000000          0
03743 020004          20004
03744 000000          0
03745 000004          4
03746 000000          0
03747 001104          1104
03750 000000          0
03751 141104          141104
03752 000000          0
03753 001104          1104
03754 000000          0
03755 141104          141104
03756 000000          0
03757 001104          1104
03760 000000          0
03761 141104          141104
03762 000000          0
03763 001104          1104
03764 000000          0
03765 000004          4
03766 000000          0
03767 000010          10
```

```
---
   03770 000000          0
   03771 140010          140010
   03772 000000          0
   03773 000010          10
   03774 000000          0
   03775 001050          1050
   03776 000000          0
   03777 013050          13050
   04000 000000          0
   04001 012010          12010
   04002 000000          0
   04003 012210          12210
   04004 000000          0
   04005 012010          12010
   04006 000000          0
   04007 000010          10
   04010 000000          0
   04011 001010          1010
   04012 000000          0
   04013 000010          10
   04014 000000          0
   04015 000210          210
   04016 000000          0
   04017 000010          10
   04020 000000          0
   04021 001110          1110
   04022 000000          0
   04023 141110          141110
   04024 000000          0
   04025 001110          1110
   04026 000000          0
   04027 141110          141110
   04030 000000          0
   04031 001110          1110
   04032 000000          0
   04033 141110          141110
   04034 000000          0
   04035 001110          1110
   04036 000000          0
   04037 000010          10
   04040 000000          0
   04041 000010          10
   04042 000001          1
   04043 000010          10
   04044 000002          2
   04045 000001          1         ;BEGIN SHORT WASH
   04046 000000          0
   04047 040001          40001
   04050 000000          0
   04051 000001          1
   04052 000000          0
   04053 001041          1041
   04054 000000          0
   04055 000001          1
   04056 000000          0
   04057 000201          201
   04060 000000          0
   04061 000001          1
   04062 000000          0
   04063 001001          1001
```

```
---
   04064 000000          0
   04065 000001          1
   04066 000000          0
   04067 000201          201
   04070 000000          0
   04071 000001          1
   04072 000000          0
   04073 001101          1101
   04074 000000          0
   04075 041101          41101
   04076 000000          0
   04077 001101          1101
   04100 000000          0
   04101 041101          41101
   04102 000000          0
   04103 001101          1101
   04104 000000          0
   04105 041101          41101
   04106 000000          0
   04107 001101          1101
   04110 000000          0
   04111 000001          1
   04112 000000          0
   04113 000004          4
   04114 000000          0
   04115 040004          40004
   04116 000000          0
   04117 000004          4
   04120 000000          0
   04121 001044          1044
   04122 000000          0
   04123 003044          3044
   04124 000000          0
   04125 001044          1044
   04126 000000          0
   04127 005044          5044
   04130 000000          0
   04131 004004          4004
   04132 000000          0
   04133 004204          4204
   04134 000000          0
   04135 004004          4004
   04136 000000          0
   04137 000004          4
   04140 000000          0
   04141 020004          20004
   04142 000000          0
   04143 021004          21004
   04144 000000          0
   04145 020004          20004
   04146 000000          0
   04147 020204          20204
   04150 000000          0
   04151 020004          20004
   04152 000000          0
   04153 000004          4
   04154 000000          0
   04155 001104          1104
   04156 000000          0
   04157 041104          41104
```

```
---
   04160 000000          0
   04161 001104          1104
   04162 000000          0
   04163 041104          41104
   04164 000000          0
   04165 001104          1104
   04166 000000          0
   04167 041104          41104
   04170 000000          0
   04171 001104          1104
   04172 000000          0
   04173 000004          4
   04174 000000          0
   04175 000010          10
   04176 000000          0
   04177 040010          40010
   04200 000000          0
   04201 000010          10
   04202 000000          0
   04203 001050          1050
   04204 000000          0
   04205 013050          13050
   04206 000000          0
   04207 012010          12010
   04210 000000          0
   04211 012210          12210
   04212 000000          0
   04213 012010          12010
   04214 000000          0
   04215 000010          10
   04216 000000          0
   04217 001010          1010
   04220 000000          0
   04221 000010          10
   04222 000000          0
   04223 000210          210
   04224 000000          0
   04225 000010          10
   04226 000000          0
   04227 001110          1110
   04230 000000          0
   04231 000010          10
   04232 000000          0
   04233 000010          10
   04234 000001          1
   04235 000010          10
   04236 000002          2
   04237 040000          40000   ;BEGIN SANITIZE
   04240 000000          0
   04241 041100          41100
   04242 000000          0
   04243 040000          40000
   04244 000000          0
   04245 040200          40200
   04246 000000          0
   04247 040000          40000
   04250 000000          0
   04251 000000          0
   04252 000000          0
   04253 001000          1000
```

```
---
   04254 000000          0
   04255 000000          0
   04256 000000          0
   04257 000000          0
   04260 000001          1
   04261 000000          0
   04262 000002          2
         000100 .BLK 100
                ;UPPER COUNTER LIMITS BUFFER
   04363 000000 ULB:     0        ;BEGIN HEAVY FABRIC
   04364 002000          2000
   04365 000000          0
   04366 000100          100
   04367 000000          0
   04370 000065          65
   04371 000000          0
   04372 001000          1000
   04373 000000          0
   04374 000035          35
   04375 000001          1
   04376 050000          50000
   04377 000002          2
   04400 070000          70000
   04401 000001          1
   04402 050000          50000
   04403 000000          0
   04404 000650          650
   04405 000000          0
   04406 003500          3500
   04407 000000          0
   04410 000020          20
   04411 000000          0
   04412 000700          700
   04413 000000          0
   04414 000025          25
   04415 000001          1
   04416 035000          35000
   04417 000000          0
   04420 000650          650
   04421 000000          0
   04422 003000          3000
   04423 000000          0
   04424 000010          10
   04425 000000          0
   04426 000750          750
   04427 000000          0
   04430 050000          50000
   04431 000000          0
   04432 011000          11000
   04433 000000          0
   04434 050000          50000
   04435 000000          0
   04436 011000          11000
   04437 000000          0
   04440 050000          50000
   04441 000000          0
   04442 011000          11000
   04443 000002          2
   04444 065000          65000
   04445 000000          0
```

```
---
  04446 001000          1000
  04447 000000          0
  04450 000100          100
  04451 000000          0
  04452 000100          100
  04453 000000          0
  04454 001000          1000
  04455 000000          0
  04456 000050          50
  04457 000001          1
  04460 000000          0
  04461 000000          0
  04462 001000          1000
  04463 000000          0
  04464 003000          3000
  04465 000000          0
  04466 000020          20
  04467 000000          0
  04470 001000          1000
  04471 000001          1
  04472 070000          70000
  04473 000000          0
  04474 001000          1000
  04475 000000          0
  04476 003000          3000
  04477 000000          0
  04500 001000          1000
  04501 000000          0
  04502 040000          40000
  04503 000000          0
  04504 012000          12000
  04505 000000          0
  04506 060000          60000
  04507 000000          0
  04510 012000          12000
  04511 000000          0
  04512 060000          60000
  04513 000000          0
  04514 012000          12000
  04515 000002          2
  04516 130000          130000
  04517 000000          0
  04520 003000          3000
  04521 000000          0
  04522 004000          4000
  04523 000000          0         ;BEGIN SHORT WASH
  04524 000300          300
  04525 000000          0
  04526 000100          100
  04527 000000          0
  04530 000150          150
  04531 000000          0
  04532 001200          1200
  04533 000001          1
  04534 170000          170000
  04535 000000          0
  04536 000700          700
  04537 000000          0
  04540 004000          4000
  04541 000000          0
```

```
---
   04542 001000          1000
   04543 000001          1
   04544 040000          40000
   04545 000000          0
   04546 000700          700
   04547 000000          0
   04550 003500          3500
   04551 000000          0
   04552 001000          1000
   04553 000000          0
   04554 043000          43000
   04555 000000          0
   04556 011000          11000
   04557 000000          0
   04560 043000          43000
   04561 000000          0
   04562 011000          11000
   04563 000000          0
   04564 043000          43000
   04565 000000          0
   04566 011000          11000
   04567 000001          1
   04570 100000          100000
   04571 000000          0
   04572 001000          1000
   04573 000000          0
   04574 000070          70
   04575 000000          0
   04576 000110          110
   04577 000000          0
   04600 001100          1100
   04601 000000          0
   04602 000050          50
   04603 000001          1
   04604 030000          30000
   04605 000002          2
   04606 060000          60000
   04607 000001          1
   04610 030000          30000
   04611 000000          0
   04612 000650          650
   04613 000000          0
   04614 003500          3500
   04615 000000          0
   04616 000020          20
   04617 000000          0
   04620 000700          700
   04621 000000          0
   04622 000025          25
   04623 000001          1
   04624 035000          35000
   04625 000000          0
   04626 000650          650
   04627 000000          0
   04630 003000          3000
   04631 000000          0
   04632 000010          10
   04633 000000          0
   04634 000750          750
   04635 000000          0
```

```
---
   04636 045000          45000
   04637 000000          0
   04640 010000          10000
   04641 000000          0
   04642 040000          40000
   04643 000000          0
   04644 011000          11000
   04645 000000          0
   04646 050000          50000
   04647 000000          0
   04650 011000          11000
   04651 000000          0
   04652 000100          100
   04653 000000          0
   04654 001000          1000
   04655 000000          0
   04656 000070          70
   04657 000000          0
   04660 000100          100
   04661 000000          0
   04662 001000          1000
   04663 000000          0
   04664 000050          50
   04665 000001          1
   04666 000000          0
   04667 000000          0
   04670 000700          700
   04671 000000          0
   04672 003200          3200
   04673 000000          0
   04674 000015          15
   04675 000000          0
   04676 001000          1000
   04677 000001          1
   04700 050000          50000
   04701 000000          0
   04702 000700          700
   04703 000000          0
   04704 003200          3200
   04705 000000          0
   04706 001000          1000
   04707 000001          1
   04710 160000          160000
   04711 000000          0
   04712 002500          2500
   04713 000000          0
   04714 004000          4000
   04715 000000          0       ;BEGIN SANITIZE
   04716 000200          200
   04717 000000          0
   04720 000020          20
   04721 000000          0
   04722 130000          130000
   04723 000000          0
   04724 001000          1000
   04725 000000          0
   04726 003500          3500
   04727 000000          0
   04730 000030          30
   04731 000000          0
```

```
---
   04732 001000          1000
   04733 000000          0
   04734 070000          70000
   04735 000000          0
   04736 001000          1000
   04737 000000          0
   04740 004000          4000
         000100 .BLK 100
```

```
---
                ;LOWER COUNTER LIMITS BUFFER
05041 000000 LLB:    0          ;BEGIN HEAVY FABRIC
05042 000700         700
05043 000000         0
05044 000065         65
05045 000000         0
05046 000045         45
05047 000000         0
05050 000600         600
05051 000000         0
05052 000015         15
05053 000001         1
05054 010000         10000
05055 000002         2
05056 030000         30000
05057 000001         1
05060 010000         10000
05061 000000         0
05062 000500         500
05063 000000         0
05064 002000         2000
05065 000000         0
05066 000000         0
05067 000000         0
05070 000550         550
05071 000000         0
05072 000005         5
05073 000001         1
05074 010000         10000
05075 000000         0
05076 000500         500
05077 000000         0
05100 002000         2000
05101 000000         0
05102 000000         0
05103 000000         0
05104 000600         600
05105 000000         0
05106 030000         30000
05107 000000         0
05110 007000         7000
05111 000000         0
05112 030000         30000
05113 000000         0
05114 007000         7000
05115 000000         0
05116 030000         30000
05117 000000         0
05120 007000         7000
05121 000002         2
05122 030000         30000
05123 000000         0
05124 000500         500
05125 000000         0
05126 000030         30
05127 000000         0
05130 000030         30
05131 000000         0
05132 000500         500
05133 000000         0
```

```
05134 000000          0
05135 000000          0
05136 130000          130000
05137 000000          0
05140 000300          300
05141 000000          0
05142 002000          2000
05143 000000          0
05144 000000          0
05145 000000          0
05146 000400          400
05147 000001          1
05150 010000          10000
05151 000000          0
05152 000300          300
05153 000000          0
05154 002000          2000
05155 000000          0
05156 000300          300
05157 000000          0
05160 030000          30000
05161 000000          0
05162 004000          4000
05163 000000          0
05164 030000          30000
05165 000000          0
05166 004000          4000
05167 000000          0
05170 030000          30000
05171 000000          0
05172 004000          4000
05173 000002          2
05174 020000          20000
05175 000000          0
05176 001000          1000
05177 000000          0
05200 001000          1000
05201 000000          0         ;BEGIN SHORT WASH
05202 000050          50
05203 000000          0
05204 000020          20
05205 000000          0
05206 000020          20
05207 000000          0
05210 000400          400
05211 000001          1
05212 120000          120000
05213 000000          0
05214 000300          300
05215 000000          0
05216 001500          1500
05217 000000          0
05220 000400          400
05221 000001          1
05222 013000          13000
05223 000000          0
05224 000300          300
05225 000000          0
05226 001500          1500
05227 000000          0
```

```
---
   05230 000400          400
   05231 000000          0
   05232 025000          25000
   05233 000000          0
   05234 006000          6000
   05235 000000          0
   05236 025000          25000
   05237 000000          0
   05240 006000          6000
   05241 000000          0
   05242 025000          25000
   05243 000000          0
   05244 006000          6000
   05245 000001          1
   05246 045000          45000
   05247 000000          0
   05250 000400          400
   05251 000000          0
   05252 000015          15
   05253 000000          0
   05254 000050          50
   05255 000000          0
   05256 000400          400
   05257 000000          0
   05260 000015          15
   05261 000001          1
   05262 017000          17000
   05263 000002          2
   05264 025000          25000
   05265 000001          1
   05266 010000          10000
   05267 000000          0
   05270 000500          500
   05271 000000          0
   05272 002000          2000
   05273 000000          0
   05274 000000          0
   05275 000000          0
   05276 000550          550
   05277 000000          0
   05300 000005          5
   05301 000001          1
   05302 010000          10000
   05303 000000          0
   05304 000500          500
   05305 000000          0
   05306 002000          2000
   05307 000000          0
   05310 000000          0
   05311 000000          0
   05312 000600          600
   05313 000000          0
   05314 025000          25000
   05315 000000          0
   05316 006000          6000
   05317 000000          0
   05320 025000          25000
   05321 000000          0
   05322 006000          6000
   05323 000000          0
```

```
05324 025000          25000
05325 000000          0
05326 006000          6000
05327 000000          0
05330 000040          40
05331 000000          0
05332 000400          400
05333 000000          0
05334 000020          20
05335 000000          0
05336 000040          40
05337 000000          0
05340 000400          400
05341 000000          0
05342 000015          15
05343 000000          0
05344 140000          140000
05345 000000          0
05346 000300          300
05347 000000          0
05350 002000          2000
05351 000000          0
05352 000000          0
05353 000000          0
05354 000400          400
05355 000001          1
05356 010000          10000
05357 000000          0
05360 000300          300
05361 000000          0
05362 002000          2000
05363 000000          0
05364 000400          400
05365 000001          1
05366 120000          120000
05367 000000          0
05370 001000          1000
05371 000000          0
05372 001000          1000
05373 000000          0         ;BEGIN SANITIZE
05374 000040          40
05375 000000          0
05376 000000          0
05377 000000          0
05400 070000          70000
05401 000000          0
05402 000400          400
05403 000000          0
05404 002000          2000
05405 000000          0
05406 000005          5
05407 000000          0
05410 000400          400
05411 000000          0
05412 030000          30000
05413 000000          0
05414 000400          400
05415 000000          0
05416 001500          1500
      000100 .BLK 100
```

• END

```
---
ASC0    003666
BIND    000053
BINO    000052
C2      003665
CHEQ1   003160
CHEQ2   003243
CHLL    003166
CN      000100
CTOK    003178
DEBA    000125
DLAY1   000147
DLAY2   000150
DSB     003705
DSBA    000120
DSBA1   000151
DSTP    003645
DSTPA   000143
HCT     000127
HCTM    000131
HDST    000106
HLL     000136
HPST    000102
HST     000104
HUL     000134
IC      003061
ICA     000111
ICB     003667
ICBA    000126
ICBA1   000152
ICN     003207
ILCT    003057
IS      003114
ISA     000113
LCT     000130
LCTM    000132
LDST    000107
LLB     005041
LLBA    000141
LLBA1   000154
LLL     000137
LOOP1   003016
LOOP2   003035
LP1A    000121
LP2A    000122
LPST    000103
LST     000105
LUL     000135
MES1    003365
MES10   003541
MES11   003556
MES12   003573
MES13   003610
MES2    003402
MES3    003417
MES4    003434
MES5    003451
MES6    003462
MES7    003477
MES8    003507
MES9    003524
```

```
---
NSCH     003037
NSCHA    000133
OFF      000110
PRST     000146
RET      003046
RET1     000123
RET2     000124
RET3     000144
RET4     000145
RS       003101
RSA      000112
SBNP     000044
SBT      000043
SDE2     000057
SN       000101
SPCL     000062
ST       003306
START    003000
STCH     003036
STCHA    000115
STE      003271
STEA     000116
STP      003625
STPA     000142
STT0     000041
TE       003313
TEA      000117
TOE      003252
TOEA     000114
ULB      004363
ULBA     000140
ULBA1    000153
```

BIBLIOGRAPHY

1. D. A. Bobroff, "Computer Controlled Testing," Automation, March 1970, p. 118-20.

2. William T. Cave and Ron G. Myers, "Automated Testing: Trends in Control and Equipment," Electro-Technology, August 1969, p. 99-105.

3. C. Clarke, "A Computer Controlled Test System for Digital Equipment," Radio and Electronic Engineer, February 1971, p. 73-6.

4. Harold T. McAleer, "A Look At Automatic Testing," IEEE Spectrum, May 1971, p. 63-78.

5. P. C. Michael, "Small Computer Speeds Circuit Testing," Electronic Engineering, December 1970, p. 56-9.

6. Matthew Fichtenbaum, "Computer Controlled Testing Can Be Fast and Reliable and Economical Without Extensive Operator Training," Electronics, January 19, 1970, p. 82-6.

7. K. J. Crook and Miss J. Blythin, "A Computer Controlled Tester for Logic Networks and a Method for Synthesizing Test Patterns," Radio and Electronic Engineer, December 1970, p. 309-15.

8. Paul M. Lee, "Practical Aspects of LSI Testing," 1971 IEEE International Convention Digest, p. 556-7.

9. Sam Hardesty, "Trends in Testing Electronic Systems," Automation, November 1971, p. 43-6.

10. Ronald P. Noonan, "Testing and Inspecting With Computers," Automation, August 1970, p. 27-31.

11. "Computerized Control of Test Instrumentation is Rapidly Approaching Near-Universal Acceptance," Electronics, January 5, 1970, p. 124-7.

12. How To Use The Nova Computers, Data General Corporation, Smithboro, Massachusetts, April 1971.

13. "Requirements For a MOS Timer/Control Device," Whirlpool Corporation, St. Joseph, Michigan, April 26, 1971.